CENG3420 Homework 1

Due: Mar. 08, 2020

Solutions

All solutions should be submitted to the blackboard in the format of **PDF/MS Word**.

Q1 (10%) The following table shows manufacturing data for one processor.

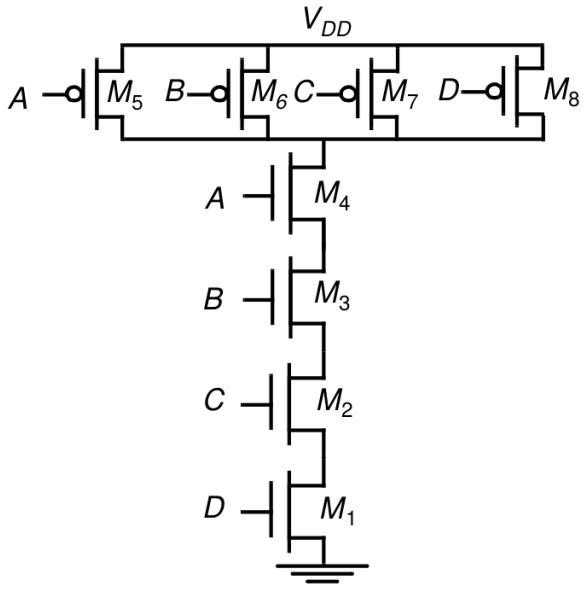
Wafer Area	Dies per Wafer	Defects per Unit Area	Cost per Wafer
200 cm^2	100	0.02 cm^{-2}	12

1. Find the yield
2. Find the cost per die
3. If the number of dies per wafer is increased by 10% and the corresponding defects per area unit is reduced by 10%, find the yield and the cost per die.

A1
1. 0.961
2. 0.125
3. 0.968, 0.113

Q2 (15%) Draw the schematic view of four-input NAND gate.

A2 As shown below.



Q3 (10%) Given a simple processor, if capacitive load is reduced by 10%, voltage is reduced by 10%, maintain the same frequency, how much power consumption can be reduced?

A3 0.271

Q4 (10%) Assume `$t0=0xAAAAAAAA, $t1=0x12345678`. Find the value of `$t2` after the following instructions, respectively.

1.
```
sll $t2, $t0, 4
or  $t2, $t2, $t1
```

2.
```
sll  $t2, $t0, 4
andi $t2, $t2, 1
```

3.
```
srl  $t2, $t0, 3
andi $t2, $t2, 0xFFEF
```

A4 As shown below,

1. 0xBABEFEF8
2. 0x00000000
3. 0x00005545

Q5 (15%) Assume that the variables a, b, c, d, and e are assigned to registers `$s0`, `$s1`, `$s2`, `$s3`, and `$s4`, respectively. Given MIPS assembly instructions:

```
sll $s2, $s4, 2
add $s0, $s2, $s3
add $s0, $s0, $s1
```

Translate the MIPS assembly instructions above into the corresponding C statement. **Please include comments for each instruction in your solution.**

A5 a = 4*e + b + d;

Q6 (15%) Assume that $a0=n and $a1=rst. Given the C statement:

```
int sum(int n, int rst){
        if (n>0)
                return sum(n-1, rst+n);
        else
                return rst;
}
```

Translate the C statement above into corresponding MIPS assembly instructions. **Please include comments for each instruction in your solution.**

A6 As shown below (assume that $a0=n and $a1=rst):

```
sum:
slti $t0, $a0, 1
bne $t0, $zero, sum_exit
add $a1, $a1, $a0
```

```
addi $a0, $a0, -1
j sum
sum_exit:
add $v0, $a1, $zero
jr $ra
```

Q7 (15%) Write down the step by step procedure to calculate 7×3 or 0111×0011. Use Multiplier0 to indicate the least significant bit of the multiplier

Iteration	Step	Multiplier	Multiplier0	Multiplicand	Product
0	Initial values	0011	1	0000 0111	0000 0000
1	1a: 1⇒Prod=Prod+Mcand	0011	1	0000 0111	0000 0111
	2: Shift left Multiplicand	0011	1	0000 1110	0000 0111
	3: Shift right Multiplier	0001	1	0000 1110	0000 0111
2	1a: 1⇒Prod=Prod+Mcand	0001	1	0000 1110	0001 0101
	2: Shift left Multiplicand	0001	1	0001 1100	0001 0101
	3: Shift right Multiplier	0000	0	0001 1100	0001 0101
3	1a: 1⇒Prod=Prod+Mcand	0000	0	0001 1100	0001 0101
	2: Shift left Multiplicand	0000	0	0011 1000	0001 0101
	3: Shift right Multiplier	0000	0	0011 1000	0001 0101
4	1a: 1⇒Prod=Prod+Mcand	0000	0	0011 1000	0001 0101
	2: Shift left Multiplicand	0000	0	0111 0000	0001 0101
	3: Shift right Multiplier	0000	0	0111 0000	0001 0101

A7

Q8 (10%) A program runs in $10s$ on computer A with 2GHz clock. If we want to design a computer B such that the same program can be finished in $7s$, determine the clock frequency of computer B. Assume it requires only $0.7\times$ clock cycles to execute the program on computer B due to different CPU design.

A8 CPU clock cycle of the program on computer A is,

$$cycle_A = 10s \times 2GHz = 2 \times 10^{10}\text{cycles}. \quad (1)$$

CPU clock cycle of the program on computer B is,

$$cycle_B = 0.7 \times cycle_A = 1.4 \times 10^{10}\text{cycles}. \quad (2)$$

Clock frequency of computer B will be,

$$cycle_B/7s = 2GHz. \quad (3)$$