# CENG3420 Homework 1

**Due**: Feb. 17, 2019

All solutions should be submitted to the blackboard in the format of **PDF/MS Word**.

**Q1** (10%) Figure 1 shows a simple multiplication algorithm in ALU design. Write down the step by step procedure to calculate $5 \times 4$ or $00000101 \times 0100$. Multiplier0 indicates the least significant bit of the multiplier.

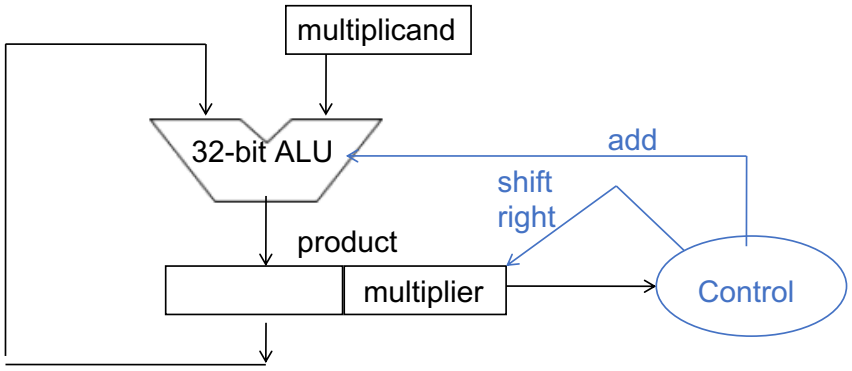


Figure 1: A simple multiplication algorithm.

**Q2** (10%) Draw the schematic view of four-input NOR gate.

**Q3** (15%) Assume `$t0=0xAAAAAAAA, $t1=0x12345678`. Find the value of `$t2` after the following instructions, respectively.

1.
```
sll $t2, $t0, 4
or  $t2, $t2, $t1
```

2.
```
sll  $t2, $t0, 4
andi $t2, $t2, 1
```

3.
```
srl  $t2, $t0, 3
andi $t2, $t2, 0xFFEF
```

**Q4** (15%) Translate the following C function into MIPS assembly (assume that $a0=n and $a1=rst). **Please include comments for each instruction in your solution.**

```
int sum(int n, int rst){
    if (n<10)
        return sum(n+1, rst+n);
    else
        return rst;
}
```

**Q5** (15%) Translate the following C implementation of Fibonacci function into MIPS assembly (assume $a0=n). **Please include comments for each instruction in your solution.**

```
int fib(int n){
    if (n==0){
        return 0;
    } else if (n==1){
        return 1;
    }
    return fib(n-1)+fib(n-2);
}
```

**Q6** (10%) Amdahl's Law defines the speedup of a processor that can be gained by using a specific feature, which is given as follows

$$S_{overall} = \frac{ExecutionTime_{old}}{ExecutionTime_{new}} = \frac{1}{(1 - Fraction_{enhanced}) + \frac{Fraction_{enhanced}}{Speedup_{enhanced}}} \quad (1)$$

Suppose that we want to enhance the processor used for Web serving. The new processor is 10 times faster on computation in the Web serving application than the original processor. Assuming that the original processor is busy with computation 40% of the time and is waiting for I/O 60% of the time, what is the overall speedup gained by incorporating the enhancement?

**Q7** (15%) Translate the following C function into MIPS assembly.

```
for (i=0; i<=100; i++)
{A[i]=B[i]+C;}
```

Assume that A and B are arrays of 64-bit integers, and C and i are 64-bit integers. Assume that all data values and their addresses are kept in memory (at addresses 1000, 3000, 5000, and 7000 for A, B, C, and i, respectively) except when they are operated on. Assume that values in registers are lost between iterations of the loop. **Please include comments for each instruction in your solution.**

**Q8** (10%) A program runs in $10s$ on computer A with 2GHz clock. If we want to design a computer B such that the same program can be finished in $7s$, determine the clock frequency of computer B. Assume it requires only 0.7X clock cycles to execute the program on computer B due to different CPU design.