CENG 3420 Midterm (2017 Spring)

Name: _____
ID: _____

Q1 (20%) Check or fill the correct answer:

1. Decimal value of 36_8 is _____.
2. Drive strength of a gate can be increased by reducing _____.
3. Name 3 instructions that can do branch _____, _____ and _____.
4. MIPS stack address grows from _____ to _____. (fill low or high)
5. As one of the evaluation metrics of computer, throughput is defined by _____.
6. A flip-flop is level-sensitive/edge-triggered.
7. Remaindor of dividing 1001011 by 1001 is _____.

Q2 (20%) Consider two different machines, with two different instruction sets, both of which have a clock rate of 200 MHz. The following measurements are recorded on the two machines running a given set of benchmark programs:

Table 1: Machine A

Instruction Type	Instructions Count	CPI
Arithmetic and logic	8	1
Load and store	4	3
Branch1	2	4
Others	4	3

Table 2: Machine B

Instruction Type	Instructions Count	CPI
Arithmetic and logic	10	1
Load and store	8	2
Branch1	2	4
Others	4	3

1. **(16%)** Determine the effective CPI, MIPS [1] rate, and execution time for each machine.
2. **(4%)** Comment on the results above.

Q3 (20%) Answer the following questions about logic gates.

1. **(8%)** Draw schematic view of NAND and NOR gates.
2. **(8%)** Considering a single bit half-adder[2]. Write the logic expressions of sum (S) and carry (C) with respective to two inputs A and B if only NAND, NOR and NOT operations are allowed.

[1] millions of instructions per second
[2] Without carry input

3. **(4%)** Based on 1 and 2, how many transistors are required to implement one-bit half adder?

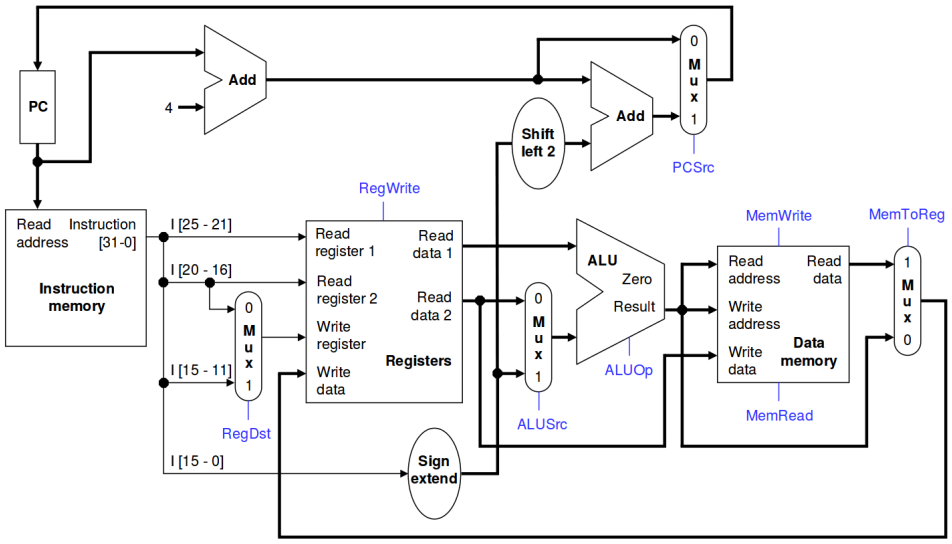
Q4 (20%) Answer the following questions about mips processor:

1. **(10%)** Elaborate five stages of load instruction in pipeline design.
2. **(15%)** Describe all possible hazards in pipeline design.
3. **(5%)** List all the data hazards of following instructions.

```
lw   $t0, 0($a0)
add  $t0, $t0, 1
sw   $t0, 0($a0)
add  $a0, $a0, 4
```

Q5 (20%) Short answer questions. Please fill in the blanks.

1. In MIPS structure, by default after one instruction, `PC` is increased by __.
2. For an R-type instruction in MIPS, the `op` field is __ bits, while the `rs` field is __ bits.
3. For a J-type instruction in MIPS, the new PC is determined by the lower ____ bits of the fetched instruction.



4. Based on the above datapath, finish the blanks in the following table. Here `lwd` is a new instruction. `lwd $rd,$rt($rs)` sets register `$rd` to the value at `Mem[$rs +$rt]`.

	RegDst	ALUSrc	MemReg	RegWr	MemRd	MemWr
`lw`	0		1		1	0
`sw`	X		X		0	1
`beq`	X		X		0	0
`lwd`	1		1			