CENG 3420 Final (Spring 2016)

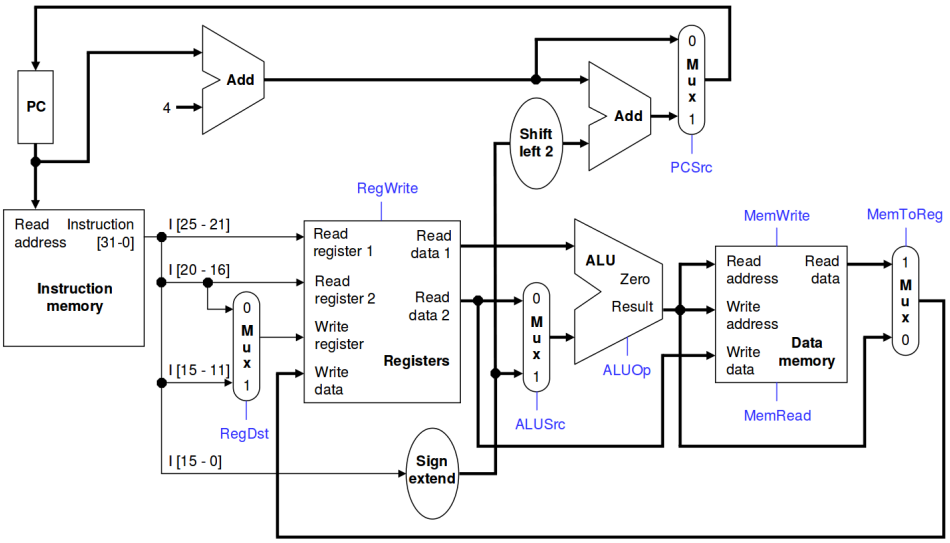
Name: _____
ID: _____

Q1 (16 marks) Short answer questions. **Circle** the right answer.

1. A conventional adder structure is Ripple Carry Adder (RCA), which is **fast / slow**. RCA consumes **lots / little** energy due to the impact of *glitching*.
2. We can detect an overflow by: Carry into MSB **xor / or / and** Carry out of MSB.
3. Intel x86 is **RISC / CISC**.
4. Stack pointer `$sp` is used to address the stack. When a data is added onto the stack, `$sp` ← **`$sp+4` / `$sp-4`**.
5. **Latch / Flip-Flop** is edge triggered, thus can be inserted between pipeline stages.
6. In pipeline, forwarding is a technique to resolve **structure / data** hazards.
7. Cache is **SRAM / DRAM** based.
8. Page Mode DRAM operation can reduce redundant **row / column** address parsing.
9. In a memory system, increasing `Tag` field length can **increase / decrease** associativity.
10. Virtual memory always use **write-back / write-through**, as it writes with speed of cache.
11. The disadvantage of I/O bus system is due to its **cost / throughput** problem.
12. To detect an I/O device, there are two methods: Port-mapped I/O (PMIO) and Memory-mapped I/O (MMIO). MIPS uses **PMIO / MMIO**.
13. There are several types of data hazards: Read After Write (RAW), Write After Read (WAR), Write After Write (WAW). **RAW / WAR / WAR** is true data dependency.
14. Shared Memory Multiprocessor (SMP) usually uses **spin-locks / message passing** for synchronization.
15. In lab2 and lab3, we are working on an **lb3c / lc3b / lb3 / lc3** simulator.

Q2 (14 marks) Short answer questions. Please fill in the blanks.

1. In MIPS structure, by default after one instruction, `PC` is increased by __.
2. For an R-type instruction in MIPS, the `op` field is __ bits, while the `rs` field is __ bits.
3. For a J-type instruction in MIPS, the new PC is determined by the lower ____ bits of the fetched instruction.



4. Based on the above datapath, finish the blanks in the following table. Here `lwd` is a new instruction. `lwd $rd,$rt($rs)` sets register `$rd` to the value at `Mem[$rs +$rt]`.

	RegDst	ALUSrc	MemReg	RegWr	MemRd	MemWr
`lw`	0		1		1	0
`sw`	X		X		0	1
`beq`	X		X		0	0
`lwd`	1		1			

Q3 (10 marks) This question is about binary representation of 8-bit number. Note that $0_{10} = 00000000_2, -1_{10} = 11111111_2$.

1. (2 marks) Calculate the binary representations of the following decimal numbers: $a = 114, b = 17, c = -73$.
2. (4 marks) Showing the details of your working, calculate using signed 8-bit binary representation for the following three sums: $a+b, b+c, a+c$. In addition, identify which case results in an overflow?
3. (4 marks) Calculate in detail using unsigned 8-bit arithmetic, the 8 bit quotient and remainder of $a \div b$.

Q4 (15 marks) Consider two processors **a** & **b**. Each processor has five stages with latencies shown in the following table. Assume that when pipelining, each pipeline stage costs **20ps** extra for the registers between pipeline stages.

	IF	ID	EX	MEM	WB
processor a	300ps	400ps	350ps	550ps	100ps
processor b	200ps	150ps	100ps	190ps	140ps

1. (4 marks) If **no** pipeline is considered, for each processor please calculate the following metrics: cycle time; latency of an instruction; the throughput. (Note that throughput is instruction number per second)
2. (4 marks) If both a & b are pipelined processors, for each one calculate the following metrics: cycle time; latency of an instruction; the throughput.
3. (7 marks) If you could split one of the pipeline stages into 2 equal halves, which one would you choose for processors a & b, respectively? For the two processors: what is the new cycle time, the new latency of an instruction, and the new throughput?

Q5 (10 marks) For a direct-mapped cache design with a 32-bit address and byte-addressable memory, consider the following two address configurations to access the cache:

	Tag	Index	Block offset	Byte offset
configuration a	$31-10$	$9-5$	$4-2$	$1-0$
configuration b	$31-12$	$11-6$	$5-2$	$1-0$

1. (5 marks) For configuration a, what's the cache line size (in words)? How many entries (cache lines) does the cache have? Note that cache lines are also called blocks.
2. (5 marks) For configuration b, what's the cache line size (in words)? How many entries (cache lines) does the cache have?

Q6 (15 marks) Consider the following instruction sequences:

```
I1: ADD R1, R2, R1
I2: LW  R2, 0(R1)
I3: LW  R1, 4(R1)
I4: OR  R3, R1, R2
```

1. (5 marks) Find all data dependences in this instruction sequence.
2. (5 marks) Find all hazards in this instruction sequence for a 5-stage pipeline with and then without forwarding.
3. (5 marks) To reduce clock cycle time, we are considering a split of the MEM stage into two stages. Find all hazards in this instruction sequence for this 6-stage pipeline with and then without forwarding.

Q7 (10 marks) Consider the following portions of two different programs running at the same time on four processors in a share memory multiprocessor (SMP). Assume that before this code is run, both x and y are 0.

Core1: `x = 2;`

Core2: `y = 3;`

Core3: `w = x + y + 1;`

Core4: `z = x - y;`

1. (8 marks) What are all the possible resulting values of w, x, y, and z? For each possible outcome, explain how we might arrive at those values.
2. (2 marks) How could you make the execution more deterministic so that only one set of values is possible?

Q8 (10 marks) This question is about Amdahl's Law:

$$\text{Speedup due to enhancement } E = \frac{1}{(1-F)+F/S}$$

where F is the fraction that can get speedup, while S is the speedup factor.

1. (5 marks) Consider an enhancement which runs 20 times faster but which is only usable 25% of the time. Calculate E.
2. (5 marks) Consider summing 100 scalar variables and two 10×10 matrices (matrix sum) on 10 processors. Calculate E.