On Reducing Both Shift and Capture Power for Scan-Based Testing

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Abstract - Power consumption in scan-based testing is a major concern nowadays. In this paper, we present a new X-filling technique to reduce both shift power and capture power during scan tests, namely *LSC-filling*. The basic idea is to use as few as possible X-bits to keep the capture power under the peak power limit of the circuit under test (CUT), while using the remaining X-bits to reduce the shift power to cut down the CUT's average power consumption during scan tests as much as possible. In addition, by carefully selecting the X-filling order, our X-filling technique is able to achieve lower capture power when compared to existing methods. Experimental results on ISCAS'89 benchmark circuits show the effectiveness of the proposed methodology.

I. Introduction

Scan-based test is the most widely adopted test strategy in the industry nowadays. It is well known, however, that an integrated circuit's power dissipation during scan test can be significantly higher than that during normal operation [2]. This brings the following problems: (i) the elevated average power consumption adds to the thermal load that must be transported away from the circuit under test (CUT) and can cause structural damage to the silicon, bonding wires, or the package; (ii) the excessive peak power dissipation is likely to cause a large voltage drop that may lead to erroneous data transfer in test mode only, thus invalidating the testing process and leading to yield loss [1].

In a full-scan circuit, it is possible that the test power consumption exceeds the circuit's power rating in both shift mode and capture mode. The power dissipations of the two operational modes, however, need to be dealt with differently. In shift mode, test vectors are shifted into/out of scan chains bit by bit, which not only dominate the test time of the CUT, but also determine the CUT's accumulated effect of test power dissipation. Therefore, our main duty in shift power reduction is to decrease the average test power dissipation *as much as possible,* so that we are able to use higher shift frequency and/or increase test parallelism to reduce the CUT's test time and hence cut down the test cost. In capture mode, since the duration is very short (typically 1 or 2 cycles per test), it has limited effect on the CUT's accumulated test power consumption. On the contrary, because test vectors are generated to detect as many faults as possible and hence often triggers more transitions in capture cycle, also because the circuit is often applied at-speed to detect delay faults and un-modeled defects, the main duty in capture power reduction is to keep it under a safe peak power limit. As long as this requirement is fulfilled, it is *not* necessary to further reduce capture power anymore.

Based on the above observation, in this paper, we propose a novel X-filling technique to reduce both shift power and capture power during scan tests, namely *LSC-filling*. The basic idea is to use as few as possible X-bits to keep the capture power under the peak power limit of the CUT, while using the remaining X-bits to reduce the shift power to cut down the CUT's average power consumption during scan tests as much as possible.

The remainder of this paper is organized as follows. Section II presents the background of low power testing. The proposed *LSC-filling* technique is described in detail in Section III. Next, we present experimental results on ISCAS'89 benchmark circuits in Section IV. Finally, Section V concludes this paper.

II. Backgrounds

A. Shift and capture power consumption during scan tests

Fig. 1 shows transitions in scan cells that cause shift and capture power consumptions during scan tests. In this circuit, the first test vector '10001' is shifted into the scan chain in five clock cycles. After one capture cycle, the response vector '00110' is captured into the scan chain and scanned out while the next test vector '01100' is scanned in simultaneously. Each vector row in this figure represents states of the scan cells in one test cycle, the dash lines highlight where transitions happen. During the shift phase, transitions on the scan chain occur when adjacent bits in test vectors have different logic values, and the number of transitions that it takes effect is determined by the position it happens. Differently, capture power is caused by transitions happened when scan cells have different values before and after capture.

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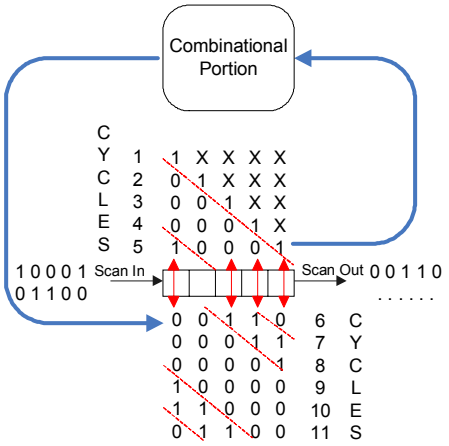


Fig 1. Shift and capture power during scan tests

B. *Prior work in low power testing*

Reducing power consumption has become an important objective of today's test development process. Prior work in this domain is mainly based on the following techniques: *scan chain manipulation, circuit modification, test scheduling, and test cube manipulation*.

Techniques based on scan chain manipulation (e.g., [3]) are very effective in reducing shift power, but usually do not help in reducing capture power. In particular, the scan chain segmentation technique is widely utilized in the industry due to the fact that it is easy to implement and highly effective in reducing shift power.

Reducing test power by modifying the circuit under test has also been proposed by several research groups. This includes clock gating [4], inserting circuitry between the scan chains and the combinational portion of the CUT to block transitions [5-7], scan enable disabling [8] and circuit virtual partitioning [9]. Circuit modification techniques are able to reduce both shift power and capture power, however, usually at a higher design-for-testability (DFT) cost.

Compared to the above DFT-based techniques, reducing test power through effective test scheduling and/or test cube manipulation methods does not incur any DFT overhead. Power-constrained test scheduling is often conducted in core-based testing, in which we carefully select embedded cores that are tested simultaneously according to a given power budget (e.g., [10]). Oftentimes only a few bits in a test pattern are essential to detect all the faults covered by it; while the remaining bits are "don't-care bits" (also known as X-bits). There are also many approaches that reduce the switching activities of the CUT by taking advantage of this property, e.g., the low-power automatic test pattern generation (ATPG) techniques in [11-13], test compression strategy in [14], and the various X-filling techniques proposed recently in [15-18].

C. *Low power X-filling*

Previous research work shows that test cubes may contain as much as 95%~98% X-bits [19]. They can be freely filled with either logic '0' or logic '1' without affecting the CUT's fault coverage. Low power X-filling techniques utilize this feature to achieve shift power and/or capture power reduction. As a totally software-based solution, these X-filling techniques do not introduce any DFT overhead and hence are easily integrated into any test flow. It should also be noted that, even if the given test cube is fully specified, the don't-care bits can still be identified with techniques such as the one proposed in [20].

Filling X-bits to reduce scan shift power is to generate fewer differences between adjacent scan cells. It is shown in [15] that logic value differences happen in different positions have different impacts on the shift power dissipation, as illustrated in Fig. 1. *Weighted Transition Metric (WTM)* is proposed to estimate shift power caused by these logic value differences. That is, the shift power in the i^{th} test vector is estimated as follows [22]:

$$WTM_i = \sum_{j=1}^{N-1} (S_{i,j} \oplus S_{i,j+1}) \times j \quad (1)$$

where N is the number of scan cells in the scan chain, $S_{i,j}$ represents the logic value of the j^{th} scan cell in this test vector. Based on this formula, [15] proposed a simple yet effective X-filling method that fills X-bits according to the logic values of their adjacent scan cells for shift power reduction, namely *adjacent fill*. For example, if the test vector is '01XX1XX0X', it is filled as '011111100', and *WTM* of this test vector is: WTM_i=2+8=10.

Filling X-bits to reduce capture power is very different from the above. The objective is to reduce the hamming distance between the input and output of every scan-FF in capture mode (denoted as the *scan capture transition count*), which is shown to be closely correlated with the circuit's switching activity. In [16], Wen et al. first presented low-capture power X-filling methodologies (denoted as *LCP-filling*) in the literature. Their method tries to reduce the scan capture transition count as much as possible by filling X-bits one by one through implication and line justification ATPG procedures. The filling order of the X-bits significantly affects the results of their approach and one of the main limitations of their method is that they try to reduce transition in a single scan cell in every filling step, without considering its effect on the other X-bits. To reduce the computational complexities of the ATPG procedures utilized in [16], Remersaro et al. introduced a probability-based X-filling technique (namely *preferred fill*) to reduce capture power [17]. However, their method is unable to weight X bits on capture power reduction efficiencies to get the optimal filling order among them.

Because of their different objectives, low-shift power X-filling techniques may result in higher capture power dissipation, and vice versa. As a result, it is necessary to consider both shift power reduction and capture power reduction during the X-filling process. [18] takes a fully specified test set as input and generates a new test set with reduced shift power and capture power. The authors first identify X-bits in the test set and then fill 50% of the X-bits using preferred fill [17] while the remaining X-bits are filled next using adjacent fill [15].

Although the X-filling procedure in [18] is able to reduce both shift power and capture power, filling half of the

X-bits for capture power reduction and the other half for shift power reduction is not a very good strategy. This is because, as discussed in Section I, the shift power dissipations and the capture power dissipation should be dealt with differently. The main objective in shift power reduction is to decrease the average test power dissipation *as much as possible,* so that we are able to use higher shift frequency and/or increase test parallelism to reduce the CUT's test time and hence cut down the test cost; while the main duty in capture power reduction is to keep it under a safe peak power limit and it is unnecessary to reduce it to be the minimum value.

Based on the above observation, the proposed X-filling methodology in this paper tries to use as few as possible X-bits to keep the capture power under the peak power limit of the CUT, while using the remaining X-bits to reduce the shift power as much as possible. This novel X-filling technique, namely *LSC-filling*, is detailed in the following section.

III. Proposed *LSC-filling* algorithm

In this section, we first present a new low-capture power X-filling scheme (namely *LC-filling*) and then detail the processing flow of *LSC-filling* that reduce both shift power and capture power. In the end, we use an example to illustrate how the proposed methodology works.

A. LC-filling for capture power reduction

The filling order of the X-bits significantly affects the CUT's capture power as many X-bits in the test responses are likely to become determined values after filling a single X-bit in the test stimulus. While in [16], the authors consider to reduce transition in each single scan cell in every filling step, we propose a novel X-filling ordering scheme for low capture power dissipation, in which we also take the X-filling effect on the other X-bits into consideration. The impact of filling one X-bit in the j^{th} scan cell for the i^{th} test vector with logic value v (i.e., '0' or '1') is calculated as:

$$T_{capture}(i,j,v) = \sum_{k\in f(v)} R_{i,k} \oplus S_{i,k} - \sum_{k\in f(v)} \overline{R_{i,k} \oplus S_{i,k}} \qquad (2)$$

where $f(v)$ represents those X-bits in the i^{th} test response that turn to be logic '0's or logic '1's after filling the test stimulus X-bit in the j^{th} scan cell into v. $R_{i,k}$ and $S_{i,k}$ are logic values of the response and the stimulus in the same scan cell.

The two terms after the equal sign in Eq. (2) denote the number of inconsistent and consistent bit pairs after filling a single X-bit, respectively, when $S_{i,k}$ or $R_{i,k}$ is 'X', both of the two items in the equation will be 0. As a result, the smaller the value of the $T_{capture}(i,j,v)$, the better to use this X-bit to reduce capture power. We use transition number on the scan chain instead of in all the node of the circuit under test to reduce the computational complexity, because there is a nearly linear relationship between these two transition numbers [22]. Based on the above, we calculate $T_{capture}(i,j,v)$ for every X-bit and sort them in a non-decreasing order. Using such X-filling order not only helps us to achieve lower capture power consumption, but also has the nice feature that the capture power can be reduced faster in the early stage of the X-filling process. This property is very helpful in our *LSC-filling* procedure (discussed next) as we can use fewer X-bits to keep the capture power under the peak power limit of the CUT.

B. LSC-filling for shift and capture power reduction

The proposed *LC-filling* technique is very effective in terms of reducing capture power with fewer X bits, but its computational time is also long. On the other hand, the computational time of low-shift power X-filling technique (we use adjacent fill [15] in this paper) is very short. Based on the above, we propose the design flow for *LSC-filling* as shown in Fig. 2.

As emphasized in the previous sections, we only need to keep the capture power within the peak power limit while we should reduce the shift power as much as possible. Therefore, in the proposed *LSC-filling* design flow, we first try to use adjacent fill for all X-bits and check whether the capture power is within the CUT's peak power limit. If not, we need to fill X-bit using *LC-filling* technique. Whenever after filling one X-bit for capture power reduction, the fast adjacent fill procedure will be conducted again to fill the remaining X-bits and then the capture power will be checked one more time to see whether this test vector still has capture power violation. If there is no violation, we have completed filling the vector; otherwise, *LC-filling* procedure is called again to reduce capture power. The above steps iterate themselves until there is no peak power violation or there is no X bit in the test cube.

C. An illustration example for LSC-filling

Fig. 3 depicts an example circuit used to illustrate our proposed *LSC-filling* procedure. There are 6 scan cells in the circuit, composing a single scan chain. To make the figure clearer, the scan cells are split into two parts: PPI pseudo-primary inputs (PPIs) and pseudo-primary outputs (PPOs), where test stimuli are shift into PPIs and test responses are captured into PPOs. The original stimuli are '10X0X1', and the responses are 'X11XX1', as shown in Fig. 3(a). We assume the peak transition limit of this scan chain is 3.

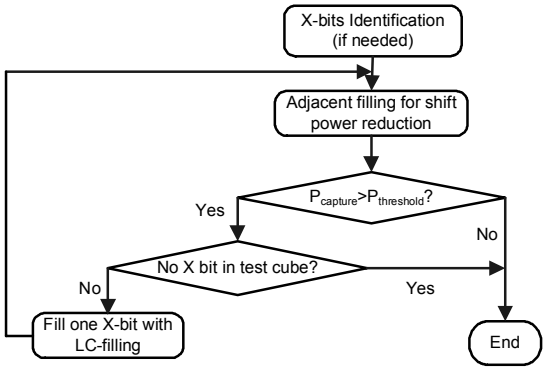
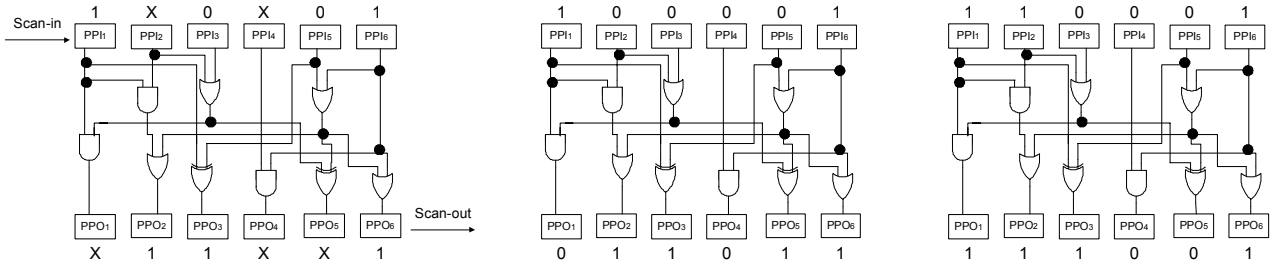


Fig 2. Proposed design flow for *LSC-filling*



(a) Original test cube (b) Adjacent fill (c) *LSC-filling* result

Fig 3. An illustration example for *LSC-filling*

Using the proposed *LSC-filling* technique, adjacent fill is conducted first, the test stimuli will become '100001', and the responses become '011011' as shown in Fig. 3(b). There will be 4 transitions during capture, which violates the peak power constraint, and hence *LC-filling* should be conducted. According to our design flow, $T_{capture}(i,j,v)$ for each X-bit in the original test vector is calculated first and we have the following values:

$T_{capture}(i,2,1) = -3;$
$T_{capture}(i,2,0) = 3;$
$T_{capture}(i,4,1) = 0;$
$T_{capture}(i,4,0) = -1$

Because $T_{capture}(i,2,1)$ is the minimum, the X-bit in PPI_2 should be the first X-bit to be filled with logic '1'. After this step, adjacent fill is conducted again and the test stimuli and responses will be as shown in Fig. 3(c). Since now there is only 1 transition during the capture cycle, which does not violate the peak power constraint of the circuit, the *LSC-filling* process for this particular vector is completed. The shift power of the new vector pair now, represented by its *WTM*, is (5+2)+(1+3)=11, it is even lower than the result of adjacent fill in Fig.2 (b), which is (5+1)+(2+3+5)=16. That is because the adjacent fill can only consider scan-in power, without optimization of the scan-out part

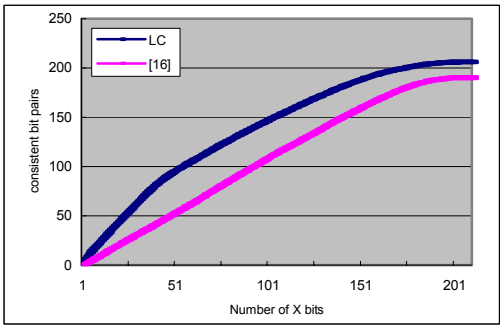
IV. Experimental Results

To evaluate the efficiency of the proposed X-filling techniques, experiments are conducted on the full-scan version of several larger ISCAS'89 circuits. MINTEST [21] is utilized to generate the test cube for these circuits.

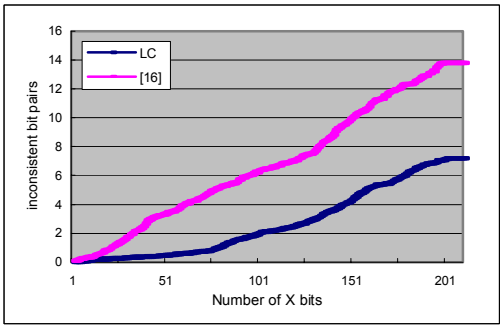
A. Experimental results for LC-filling

We first compare our *LC-filling* technique with the *LCP-filling* method proposed in [16], in which *LC-filling* fills X-bits in the test cube guided by the $T_{capture}(i,j,v)$ values. Table I compares the number of capture transition in scan cells after applying the two X-filling methods. The number of scan cells and the number of test patterns for each circuit are listed under "# of Scan Cells" and "# of Patterns"; while the scan capture transition counts after applying *LCP-filling* and *LC-filling* are shown under "LCP" and "LC", respectively. From this table, we can observe that for the three small benchmark circuits, *LC-filling* results in the same capture transition count as in [16]; while for the remaining larger benchmark circuits, the proposed method can achieve more capture power reduction when compared to [16].

To show the effect of the optimal X-filling order in *LC-filling*, the X-bits filling progress for benchmark circuit s9234 is depicted in Fig. 4, in which Fig. 4(a) shows the growth of consistent bit pairs as filling more X bits; while Fig. 4(b) presents the growth of inconsistent bit pairs at the same time. A consistent bit pair is a pair of test stimulus and response bit for a scan cell that have the same logic values, which means this scan cell will not switch in the capture cycle. An inconsistent bit pair is the opposite and implies capture power dissipation.



(a) Growth of consistent bit pairs



(b) Growth of inconsistent bit pairs

Fig 4. Observation of filling progress for s9234

TABLE I
Capture power reduction of proposed method and [16]

Circuits	# of Scan Cells	# of Patterns	LCP[16]	LC	reduction
s1196	18	139	1	1	0
s1238	18	152	1	1	0
s5378	179	111	26	26	0
s9234	211	159	26	19	26.92%
s13207	638	236	37	25	32.43%
s15850	534	126	31	22	29.03%
s38417	1636	99	185	136	26.49%
s38584	1426	136	152	130	14.47%

From Fig. 4(a), we can observe that filling an X-bit with the proposed *LC-filling* technique lead to more consistent bit pairs than using *LCP-filling* [16]. In fact, since *LCP-filling* reduces transition in a single scan cell without considering its impact on other X-bits, the consistent bit pairs grows nearly in linear. By carefully selecting the X-filling order, our *LC-filling* achieves much higher consistent bit pairs' growth speed at the early X-filling stage. For example, in this figure, it requires to fill close to 100 X-bits for [16] to obtain 100 consistent bit pairs, while it only costs *LC-filling* about 50 X-bits to achieve the same objective. Similarly, as can be seen in Fig. 4(b), the growth of inconsistent bit pairs in *LC-filling* is in a much slower pace when compared to the one in *LCP-filling* in the beginning phase. Due to the above, we can use much fewer X-bits to fulfill the CUT's peak power constraint when filling them for capture power reduction, which greatly facilitate us to achieve the optimization goal in the *LSC-filling* process.

B. Experimental results for LSC-filling

In Table II, we show comparison among three X-filling techniques: *adjacent fill*, *LC-filling* and *LSC-filling*, in terms of both shift power and capture power. The CUT's peak power constraint is set as 30% of the total number of scan cells, i.e., fewer than 30% of the scan cells are allowed to switch in capture cycles. It can be observed the initial test cube for several benchmark circuits contain capture power violations, which cannot be resolved through X-filling techniques. Inside the table, "*Ave. Shift*", "*Ave. Cap.*", "*Max. Cap.*", and "*# of Vio.*" represent the average shift power dissipation measured by its *WTM*, the average capture transition count, the maximum capture transition count, and the number of peak power violations, respectively.

From Table II, we can see that, *adjacent fill* results in much lower shift power dissipation when compared with *LC-filling*, but it also causes much more power violations during the capture phase. At the same time, with *LC-filling*, the average capture power is reduced significantly. This is however unnecessary as emphasized in previous sections that it is satisfying as long as the maximum capture power dissipation is within the circuit's peak power limit. With the proposed *LSC-filling*, we can observe the average capture power dissipation is much higher than the case in *LC-filling* (similar to the *adjacent fill*), but the maximum capture power dissipation is close to the value obtained using *LC-filling*. We also get the same number of peak power violations for all benchmark circuits. This is expected because we use only a few X-bits to control capture power and the other X-bits for shift power reduction. In addition, we can see in Table II that similar shift *WTM* values as *adjacent fill* is achieved. There are a few exceptions that we got even lower shift power and we attribute them to the inherent inaccuracy of the greedy heuristic. The computational time of the *LSC-filling* method depends on whether the capture power constraint is stringent, in our experiments it is in the same range as in [16].

Finally, since X-filling techniques as a software-based solution, it is compatible with other DFT-based low test power solution. We combine it with the scan segmentation technique proposed in [3] to see their compound effect. Fig.5 presents the average shift and capture power, and the number of vectors that have peak power violation for benchmark circuit s15850 under three configurations: 1) Random: X-bits are filled randomly, and there is only one scan chain in the circuit; 2) Segmented: X-bits are filled randomly, and the scan cells are segmented into 3 scan chains; 3) *LSC-filling* with scan segmentation: X-bits are filled with *LSC-filling*, and the scan cells are segmented into 3 scan chains. From this figure, we can observe that, while scan chain segmentation can greatly reduce average shift power of the CUT, it cannot reduce the capture power and causes capture power violations in many test vectors. Together with *LSC-filling*, these violations are eliminated. Moreover, it can further reduce average shift power to about half of that under the "Segmented" configuration. As a result, the combined solution not only facilitates the reliability of the test, but also allows us to use higher shift frequency during test and/or enhance the test parallelism of the CUT, thus leading to low-cost test solutions.

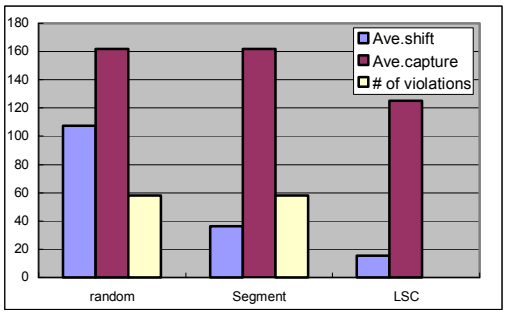


Fig 5 *LSC-filling* vs. scan chain segmentation for s15850

TABLE II

X-filling comparison in terms of shift power and capture power reduction

Circuits	# of Vio.	Adjacent fill				LC-filling				LSC-filling			
		Ave. Shift	Ave. Cap.	Max. Cap.	# of Vio.	Ave. Shift	Ave. Cap.	Max. Cap.	# of Vio.	Ave. Shift	Ave. Cap.	Max. Cap.	# of Vio.
s1196	2	**69**	9	14	132	134	**1**	**8**	**2**	117	3	**8**	**2**
s1238	4	**70**	9	14	147	135	**1**	**7**	**4**	118	3	**7**	**4**
s5378	10	**5976**	87	119	111	11337	**26**	**93**	**15**	9761	51	**93**	**15**
s9234	0	**13537**	75	104	126	19660	**19**	**59**	**0**	14924	60	62	**0**
s13207	0	92235	214	289	178	147895	**25**	**184**	**0**	**84035**	168	190	**0**
s15850	0	63975	135	236	25	69734	**22**	**127**	**0**	**58481**	125	159	**0**
s38417	0	**391913**	334	541	7	677308	**136**	**350**	**0**	391989	330	489	**0**
s38584	0	**489613**	375	700	7	795848	**130**	**487**	**1**	492169	365	**487**	**1**

V. Conclusion

In this paper, we present a novel X-filling technique namely *LSC-filling* to reduce both shift power and capture power during scan tests. The basic idea of our proposed technique is to use as few as possible X-bits to keep the capture power under the peak power limit of the CUT, while using the remaining X-bits to reduce the shift power to cut down the CUT's average power consumption during scan tests as much as possible. In addition, by carefully selecting the X-filling order, our X-filling technique is able to achieve lower capture power when compared to existing methods. Experimental results on ISCAS'89 benchmark circuits show that *LSC-filling* is able to achieve low shift power while fulfilling the peak power requirement during capture.

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