Modeling TSV Open Defects in 3D-Stacked DRAM

Li Jiang[†§], Yuxi Liu[†], Lian Duan[‡], Yuan Xie[‡], and Qiang Xu[†§]

[†]CUhk REliable computing laboratory (CURE)
Department of Computer Science & Engineering
The Chinese University of Hong Kong, Shatin, N.T., Hong Kong
[§]Shenzhen Institutes of Advanced Technology, Chinese Academy of Sciences
Email: {ljiang,yxliu,qxu}@cse.cuhk.edu.hk

[‡]Department of Computer Science & Engineering
Pennsylvania State University, USA
Email: {duan,yuanxie}@cse.psu.edu

Abstract

Three-dimensional (3D) stacking using through silicon vias (TSVs) is a promising solution to provide low-latency and high-bandwidth DRAM access from microprocessors. The large number of TSVs implemented in 3D DRAM circuits, however, are prone to open defects and coupling noises, leading to new test challenges. Through extensive simulation studies, this paper models the faulty behavior of TSV open defects occurred on the wordlines and the bitlines of 3D DRAM circuits, which serves as the first step for efficient and effective test and diagnosis solutions for such defects.

1 Introduction

Three-dimensional (3D) die-stacking technology has recently received a great deal of attention in both industry and academia [20, 25]. By bonding planar circuit layers at micrometer distances with low-latency, high-bandwidth and dense through-silicon vias (TSVs), 3D technology offers many benefits over traditional 2D designs, e.g., shortened global interconnects and integration of disparate technologies. In particular, stacking DRAM circuits on top of a processor is shown to be a promising solution to tackle the well-known "Memory Wall" problem in the computer architecture community [6].

3D-stacked memories can be implemented in several manners. One possible organization is simply using TSVs to implement a vertical bus across multiple DRAM layers to link them to the processor layer [5, 16, 24], as shown in Fig. 1(a). Such memory organization reduces the long memory access latency, but does not provide much bandwidth benefits because the individual structures in each layer are still traditional two-dimensional memory structures.

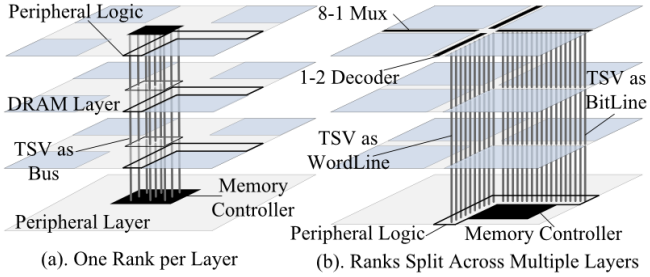

Figure 1. 3D-stacked DRAM.

To fully exploit the benefits of 3D stacking technology, another DRAM organization is introduced wherein individual storage-cell arrays are stacked in a 3D fashion. TSVs are used to link these memory arrays from different layer to peripheral logic (e.g. decoder and sense amplifier) in bottom layer [6], as shown in Fig. 1(b). By isolating the peripheral logic implemented with CMOS technology from the DRAM bit-cells implemented with NMOS technology, such architecture not only reduces manufacturing complexity, but also enables individual optimizations of logic layer for speed and storage-cell layers for density, thus dramatically reducing memory access time. In addition, TSVs are implemented as part of the bitlines and wordlines, leading to significant increase of memory bandwidth.

Recently, Tezzaron Semiconductor has implemented the above "true" 3D DRAM architecture (see Fig. 1(b)). In their design, one TSV is shared by two wordlines through a 1 to 2 decoder at the edge of each memory array. At another edge of each memory array, 8 to 1 multiplexors are placed to control which bitline can connect to the sense amplifier by TSV [15]. This design not only reduce the number of TSVs, but also relieves the pitch-mismatch problem [15]. Even with the above design, such DRAM organization still leads to a massive us-

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age of TSVs with density in the range of tens of thousands of TSVs/mm^2, that is, approximately 1.5 million TSVs for 1Gb memory [10]. Consequently, to obtain high manufacturing yield for such 3D DRAM circuits, it is essential to understand the faulty behavior of TSV defects and develop effective test and repair solutions to tolerate such defects.

The primary failure mechanism for TSVs is random open defects (e.g., caused by void after filling) during TSV fabrication [12]. However, we cannot simply model such defects as wordline/bitline stuck-open faults as in [17] for 2D memory circuits. This is because, the extremely high density of TSVs makes capacitive coupling effects among them not negligible [11]. To tackle this problem, in this paper, we conduct extensive simulations to study the faulty behavior of TSV open defects and map them to functional fault models of the memory circuits, which serves as the first step to tackle the test and repair problem for 3D DRAMs.

The remainder of this paper is organized as follows. Section 2 presents preliminaries of this work. In Section 3, we describe the simulation methodology employed in this work. Next, the simulation results and analysis for wordline opens and bitline opens due to TSV defects are detailed in Sections 4-5. In Section 6, we extend our simulation study by considering the TSV coupling effects from multiple silicon layers in the DRAM. Then, we map the TSV open defect into memory functional fault models and present corresponding test implications in Section 7. Finally, Section 8 concludes this paper.

2 Preliminaries

2.1 Memory Operation

Fig. 2 presents an example equivalent circuit with one DRAM layer connecting to the bottom peripheral layer using TSVs. For simplicity, only three wordlines (WL_0-WL_2) are shown in this figure. With the commonly-used folded bitline DRAM architecture [4], each column in the memory array has two bitlines (BL and $\overline{BL}$), intersecting each wordline at two points, wherein one storage-cell is placed in one of these two points. Nevertheless, the storage-cell can be placed in either BL or $\overline{BL}$, for example, storage-cells along WL_0 are all in $\overline{BL}$ ($\overline{BL_i}$,$\overline{BL_{i+1}}$,...) while those along WL_1 and WL_2 are all in BL (BL_i,BL_{i+1},...) (see Fig. 2). Pass transistor connects storage-cell with bitline, and it is controlled by the corresponding wordline.

During write operation, the wordline is driven with logic '1', turning on the pass-transistor. After write enable signal (WE) is turned on, the input data directly drives the bitlines (e.g., drives BL to '1' and drives $\overline{BL}$ to '0' simultaneously), charging (discharging) the target cell capacitor. During read operation, there are four phases: (i) In *precharge* phase, both BL and $\overline{BL}$ are charged as V_{ref} by precharge circuit. After that, precharge circuit is isolated from bitlines. (ii) In *access* phase, a specific wordline is accessed by driven to logic '1, turning its pass-transistors on. Then the storage-cell capacitors begin to charge/discharge the BL while $\overline{BL}$ remains as V_{ref} (i.e. when WL_1 or WL_2 is accessed in Fig. 2), and vice versa (i.e. when WL_0 is accessed). (iii) In *sensing* phase, the minute voltage difference between BL and $\overline{BL}$ makes the two transistors in diagonal position in sensing circuit more conductive, leading to a positive feedback, which continually enlarges the voltage difference until one of them is pulled up to '1' while the other dragged down to '0'. (iv) Finally, the result comes out through the output circuit and is restored back to the accessed storage-cell.

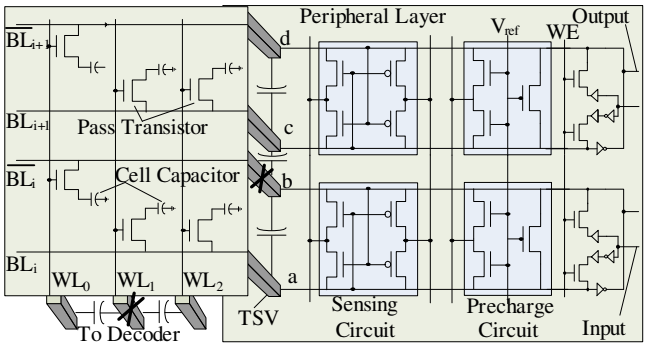


Figure 2. 3D DRAM Model.

2.2 Related Work and Motivation

Open defect can be classified as full open defect and resistive open defect. In [17], full open defects in memory circuits are modeled as stuck-open faults. With this fault model, when an open spot occurs on the wordline/bitline, the memory cell becomes unaccessible. Resistive open defects on the wordlines/bitlines of traditional 2D DRAM circuits have also been extensively studied in prior works [27, 28] using defect injection and SPICE simulation [3, 21]. Various address fault models (AFs) have also been proposed to target full open defects in the address decoders [2, 22].

Generally speaking, a full open defect breaks an interconnect into two parts: one connected to the source, while the other disconnected as a floating net. According to several electrical models for full interconnect opens [9, 14, 26], the parasitic capacitances between the floating net and its neighbors may have a significant impact on the voltage of the floating part, and *Aggressor-Victim* model is commonly used for analysis. For example, in [26], the authors sum up all the coupling capacitance of aggressors having logic value '0/1' as C_0/C_1. Then it determines the voltage of the floating part by comparing C_0 and C_1.

When TSVs are used as part of the wordlines/bitlines in 3D DRAMs, however, not only they are more prone to random open defects [12], but also their capacitive coupling is more severe when compared to their counterpart in 2D memory, as studied in [11]. Previous open fault models hence cannot accurately capture the faulty behavior of TSV open defects in 3D DRAM. In addition, as the coupling effects between aggressor TSVs and victim TSV vary with the operation of the DRAM, the faulty behavior of TSV open defects in 3D DRAM is affected by many factors, e.g., operation type (i.e., read or write), voltage of its neighboring wordlines/bitlines and coupling capacitance from its surroundings.

Consequently, it is almost impossible to analyze the faulty behavior of such defects statically. The above motivates us to conduct extensive simulations to study TSV open defects. In particular, we focus on full TSV open defects in this work.

3 Simulation Methodology

Based on [6], we set the size of TSV as $1.5\mu m \times 1.5\mu m$. According to the 3D DRAM cell feature size and the TSV used in wordline/bitline, we estimate the distance between TSVs to be $2-4\mu m$, considering the TSV sharing mechanism mentioned earlier. The parasitic parameters for TSVs are set according to [11], and two reasonable values $0.6fF$ and $1fF$ are assumed as the boundary of their coupling capacitance in our simulation, regardless of the TSV open position. The storage-cell intrinsic capacitance is set to be $30fF$. We also set $V_{dd} = 1.8V$ and reference voltage as half of it. The threshold voltage of each pass-transistor is set to be $0.5V$. Thus, to simulate logic '1' in accessed cells, we set the initial value to be $1.3V$, the maximum voltage can be written into a cell.

In our simulation study, for a victim TSV with an open defect, we only consider the capacitive coupling effects from its neighboring TSVs, because the coupling effects from farther TSVs are usually shielded out by the TSVs in between [11]. We are not concerned about the coupling effects between TSVs used to implement part of wordlines and those on bitlines. This is because they are routed outside of two different borders of each DRAM bank respectively, and hence their coupling effects can be ignored. In addition, we differentiate TSVs that are at the border with neighbors at only one side (denoted as *border TSVs*) and TSVs that are in the middle and hence are surrounded by other TSVs (denoted as *middle TSVs*), because they suffer from different coupling effects. For the ease of discussion, we denote "Y**w**X" as write logic X (i.e., '1' or '0') to a cell with logic Y ('1' or '0'). Similarly, "X**r**" denotes read from a cell with logic X. We also assume that the coupling effect between TSVs and traditional vias are negligible due to the small size of traditional vias. Since "0**w**0" and "1**w**1" operations do not change the cell capacitor, we only consider the following operations: "1**w**0", "0**w**1", "1**r**", and "0**r**" in our simulation.

The simulation studies conducted in this work are summarized in Table 1. Simulation for bitline with TSV open defects is rather simple since all the bitlines within a block are accessed in any write or read operation. In other words, BL_o and the neighboring bitlines of the BL_o are accessed at the same time. For simulation on wordline with TSV open defect, however, we need to differentiate the case for accessing the wordline with open defect and that for accessing the neighbor of the wordline with open defect. In the following, we first show our simulation models and results for wordline/bitline opens considering coupling effects from TSVs originating from the same layer, where there are at most two neighboring aggressors to the floating wire (Section 4-5). Then, in Section 6, we extend the simulation model to consider coupling effects between TSVs passing through different layers.

Open Position	Operation	Mode	Setup	Result Analysis
wordline with TSV open defect(WL_o)	access WL_o	-	-	-
	access neighbor of WL_o	write	wordline load capacitance	two cases for middle TSV open and border TSV open
				two cases for write one time and write multiple times
		read	voltage built by trapped charges	two cells in the same bitline and in complemental bitlines
bitline with TSV open defect (BL_o)	access BL_O and its neighbors	write	-	-
		read	-	compatible coupling and competitive coupling

Table 1. Summary of Applied Simulation.

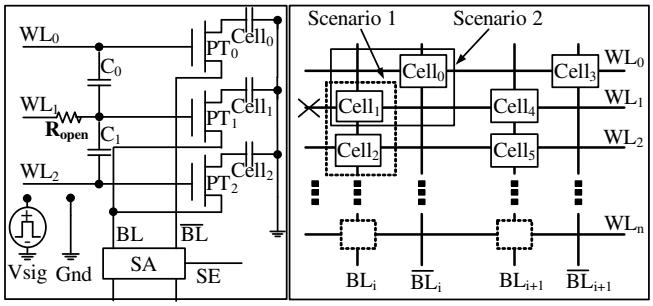
4 Simulation for Wordline Opens

4.1 Simulation Setup

For TSV open defect on wordline, the floating part is the wordline in DRAM layer and the pass transistors (MOSFET) on it. According to [14], the gate-to-source voltage (V_{gs}) of a floating pass transistor depends on three factors: voltage on neighboring nets of the floating wordline (V_{mg}), the drain-to-source voltage (V_{ds}) that determines the operational region of transistor (i.e., off, linear or saturation), and the trapped charges deposited during fabrication on the floating gate of pass-transistor [8]. As we are not certain about the amount of trapped charges on a particular interconnect open, in this work, we investigate the faulty behavior by varying the voltage built up on floating gate of pass-transistor by trapped charges.

Let us consider the example circuit in Fig. 2 and suppose WL_1 has a TSV open defect, there are two possible cases to be concerned: (i) WL_1 is accessed (turned on); (ii) one of WL_1's neighbors, e.g., WL_2, is accessed. For the former case, as none of its neighbors can be turned on (only one wordline can be accessed in a memory bank), it behaves as a stuck-open fault and we can map it to existing addressed fault models [2, 17]. We therefore only need to simulate for the latter case (see Table 1).

Fig. 3(a) shows the schematic circuit used in our simulation for wordline opens. The open defect is represented by a very large resistance R_{open} in SPICE simulation. Wordline WL_1 has an open TSV, and we simply denote it as an *wordline with open defect*. Wordline WL_0 (WL_2) is the neighboring wordlines. PT_0-PT_2 are the pass transistors. C_0 and C_1 are the corresponding coupling capacitance between adjacent TSVs. $Cell_1$ is the *floating cell* while $Cell_0$ is the *accessed cell* when WL_0 is turned on ($Cell_2$ becomes the *accessed cell* when WL_2 is turned on). The wire parasitic capacitance in wordline and bitline (C_w and C_b) are not shown in schematic for clarity. We use a voltage pulse source (V_{sig}) to represent the voltage change. Thus an accessed wordline connects V_{sig}, while those wordlines turned off connect Gnd. There are two scenarios in terms of the corresponding position between floating cell and accessed cell: (i) the accessed cell ($Cell_2$) and floating cell ($Cell_1$) are in the same bitline; (ii) the accessed



(a) Schematic for Wordline Open (b) Two Scenarios for Wordline Open

Figure 3. Simulation Model for Write/Read Operation with Wordline Opens.

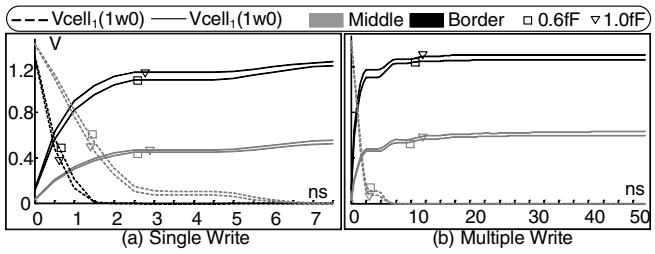


Figure 4. Write Operation with Wordline Open when Wordline Load Capacitance is $10fF$.

cell ($Cell_0$) and floating cell ($Cell_1$) are in the complemental bitlines. We use the following example to demonstrate these two scenarios.

Fig. 3(b) presents the structural view of accessing neighboring wordline of an open one. Let us consider wordline (WL_1) is open, thus $Cell_1$ is the floating cell. For scenario (i), WL_2 is accessed and $Cell_2$ is the accessed cell. $Cell_1$ and $Cell_2$ are in the same bitline (BL_i). For scenario (ii), WL_0 is accessed and $Cell_0$ is the accessed cell. $Cell_0$ and $Cell_2$ are in complemental bitlines.

During the write operation there is no difference between these two scenarios, since there is a source driving both *BL* and $\overline{BL}$. Thus, we turn off the sense enable signal *SE* to isolate the sensing amplifier and drive the bitline *BL* to corresponding logic (logic '1" or logic '0') (see Fig. 3(a)). During read operation, the corresponding position of the accessed cell and floating cell should be considered, because there is no strong source in bitline during sensing phase. Thus, the different corresponding positions of the accessed cell and the floating cell affect the simulation results. As a result, we consider both scenarios when conducting simulations for read operation on wordline with open defect.

4.2 Simulation Results and Analysis for Write Operation

This section presents the result of write operation by accessing neighboring wordline of the wordline with open defect (see Table. 1). Both middle TSV with open defect and border TSV with open defect are considered. Furthermore, we conduct simulation studies for both single write operation and multiple write operations. As wordline load capacitance significantly affects simulation results, to further investigate the impact of wordline with TSV open defects, we vary the wordline capacitance from $1fF$ to $200fF$ in our simulation.

Fig. 4(a)-(b) shows voltage change on $Cell_1$ due to the coupling effect between accessed wordline and wordline with open defect when we set the C_w as $10fF$. As can be observed from Fig. 4(a), for *middle* TSV open, a single "0**w**1" operation to $Cell_1$ can only drive $Cell_0$ to $0.4V$ due to the weak pulling up capability of NMOS transistor while the "1**w**0" operation can pull down the voltage of $Cell_0$ efficiently. On the other hand, Fig. 4(b) shows the simulation results by applying the same operation six times (i.e., "0**w**1**w**1**w**1**w**1**w**1**w**1" and "1**w**0**w**0**w**0**w**0**w**0**w**0"). For wordline with *middle* TSV open, the voltage can be written into a cell capacitor in "0**w**1" operation is no more than $0.6V$, while the times needed to write cell capacitor to 0 depends on the coupling capacitance because aggressor TSVs with higher coupling capacitance is more effective to drive the floating cell capacitor. Both Fig. 4(a)-(b) show that they are able to drive cell capacitor in a *border* TSV more aggressively, even with low coupling capacitance $0.6fF$.

When the load capacitance of wordline is larger than $50fF$, our simulation results show that the voltage change of the wordline with open defect is negligible, forcing the pass-transistor in off mode. As a result, the write operation on neighboring wordline of the wordline with TSV open defect cannot change the voltage of the floating cell.

4.3 Simulation Results and Analysis for Read Operation

This section presents the result of read operation by accessing the neighbor of the wordline with open defect (see Table. 1). Both scenarios wherein the floating cell and accessed cell are in the same bitline or in complemental bitlines are considered. Previous results show that a wordline with open defect cannot turn on the pass-transistor when its neighboring wordline are accessed with large load capacitance. However, we cannot simply conclude that the coupling effect between the accessing wordline and the wordline with TSV open defect has no impact on read operation. This is because another important factor of interconnect open, i.e., trapped charges deposited during fabrication on gate of pass-transistors could build up enough voltage (gate-to-source voltage V_{gs}) so that the floating cell is accessible [7, 18].

Because of this, two storage-cells may be read out at the same time. One is in the accessed wordline (accessed cell) while the other is in the wordline with open defect (floating cell). To investigate the impact of trapped charges on the gate of pass-transistor, we vary the initial voltage (V_{trap}) on floating gate of pass-transistor during our simulation.

The simulation study shows that there are two scenarios that the output is affected by a floating cell: (i) when the

floating cell and the accessed cell are in the same bitline, and accessed cell is with logic '1' while the floating cell is with logic '0'; An example corresponding to this scenario is accessing WL_2 while $Cell_1 = 0$ and $Cell_2 = 1$ in Fig. 3(b); (ii) when the floating cell and the accessed cell are in complemental bitlines, and the two cells are both with logic '0'. An example corresponding to this scenario is accessing WL_0 while $Cell_0 = 0$ and $Cell_1 = 0$ in Fig. 3(b). By varying V_{trap}, we observe the faulty behavior of scenario (i) when $V_{trap} \geq 0.7V$ (see Fig. 5(a)) and the faulty behavior of case (ii) when $V_{trap} \geq 1.0V$ (see Fig. 5(b)), respectively. Fig. 5(a)-(b) present the corresponding results of cells staying in the same bitline and the complemental bitline, respectively. The curves in both figures start at the time when the pass-transistors are turned on (denoted as '*wordline access*') and the sense phase (denoted as '*SA*') starts 5*ns* after 'word access' (see Fig. 5). In both cases, faulty behavior can be observed when coupling capacitance varies from $0.6fF$ to $1fF$.

In Fig. 5(a), $Cell_1$ and $Cell_2$ are fighting with each other on the same bitline after wordline access. Bitline is first discharged by $Cell_1$, leading to voltage drop. Then, the charging effect from $Cell_2$ becomes dominant and pulls up the voltage of bitline. However, it cannot reach V_{ref} at last, leading to incorrect result. The correct voltage of BL_i should be logic '1' but now it is logic '0'. The correct voltage of $Cell_2$ should be logic '1' (the voltage in accessed cell remains the same during read operation due to the restore phase), but now it is also logic '0'. The voltage of $Cell_1$ remains the same as logic '0'.

In Fig. 5(b), $Cell_0$ and $Cell_1$ are fighting on two complemental bitlines, which are being discharged from V_{ref} ($0.9V$). Along with the charging process from bitline to storage-cell capacitor, the voltage of storage-cells increases while the voltages in bitline decrease. Thus, V_{ds} of pass transistor (equal to voltage difference between bitline and cell capacitor) is reduced. The charging process ends when it achieves a balance situation wherein the voltage of cell is approximately equal to the bitline voltage. At this time, however, it is not strong enough to charge the floating cell $Cell_1$ from logic '0' to logic '1', because the gate conductivity of floating cell is weaker than that of the accessed cell ($Cell_0$). Thus, during the sense phase (5*ns* after wordline access), the voltage in BL_i is lower than that in $\overline{BL_i}$, amplified by sense amplifier, leading to incorrect result. The correct voltage of $\overline{BL_i}$ should be logic '0', but now it is logic '1'. The correct voltage of $Cell_0$ should be logic '0', but now it is also logic '1'. The voltage of $Cell_1$ remains the same as logic '0'.

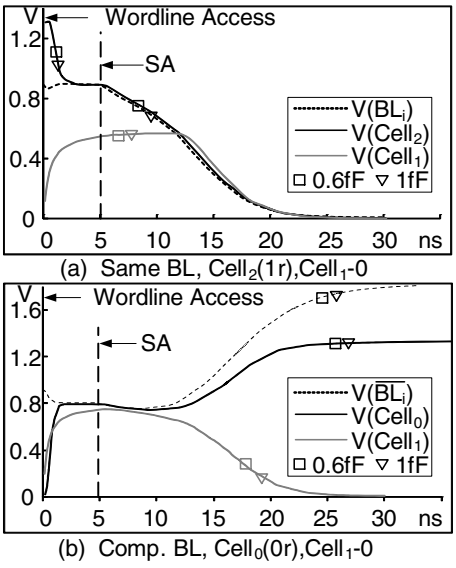


Figure 5. Read Operation with Wordline TSV Open.

5 Simulation for Bitline Opens

5.1 Simulation Setup for Bitline Opens

Fig. 6 presents the schematic circuit used in our simulation for bitline BL_i with TSV open defect. The coupling capacitance C_c is between adjacent TSVs. The simulation setup for write operation is less complicated, because sense amplifier is shut down during write operation, and only the storage-cells along with accessed wordline are affected. To simulate '0w1', we link a voltage pulse source to the corresponding bitline, and we connect the bitline with the ground to simulate '1w0'. During read operation, all bitlines are floating and at V_{ref} between the end of pre-charge phase and the beginning of sensing phase. We present the simulation results from the sensing phase. All the bitlines are charged/discharged by their storage-cells except the bitline with open TSV defect, and the coupling effect is investigated in our simulation.

5.2 Simulation Results and Analysis for Write Operation

For write operation on bitline with open TSV defect, we find that the voltage change in storage-cell in the bitline with open defect is negligible, by driving logic '1' or logic '0' respectively to all bitilnes. If the initial voltage of the accessed cell in open bitline is logic '0', no matter what logic is written into these bitlines, the voltage of storage-cell remains near to $0V$. If the initial voltage of the accessed cell in open bitline is logic '1', no matter what logic is written into these

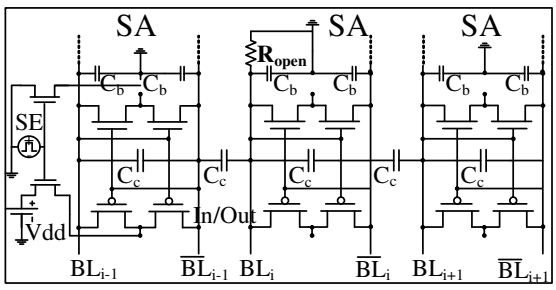


Figure 6. Simulation Model for Write/Read Operation with Bitline Opens.

bitlines, the voltage of storage-cell is reduced dramatically. This is because, comparing to the large parasitic capacitance in the bitline, the coupling effect from neighboring bitlines is negligible. In addition, the sense amplifier is shut down during write operation. As a result, the voltage drop in accessed cell is caused by discharging from accessed cell to parasitic capacitance of the open bitline. In practice, both write operations on open bitline and its neighbors do not change the behavior of the open bitline.

5.3 Simulation Results and Analysis for Read Operation

Suppose bitline BL_i suffers from TSV open defect in an example circuit shown in Fig. 7. For read operation with BL_i, let us consider two cases: (i) If we access WL_0, bitline $\overline{BL_i}$ is driven by $Cell_3$. Although bitline BL_i is floating with reference voltage due to open defect, the sense amplifier can still sense the voltage difference between $\overline{BL_i}$ and BL_i and then drive both bitlines to opposite voltages. In this case, the open defect does not influence the output of read operation. (ii) If we access WL_1, bitline $\overline{BL_i}$ is floating because there is no storage-cell being accessed in $\overline{BL_i}$. At the same time, bitline BL_i is also floating due to the TSV open defect. Thus, bitline BL_i is indirectly influenced by $Cell_1$ on bitline BL_{i-1} via the neighboring bitline $\overline{BL_{i-1}}$ while bitline $\overline{BL_i}$ is directly influenced by $Cell_7$ on bitline BL_{i+1} (see the arrows in Fig. 7). As a result, we run simulation for the latter case to see the corresponding faulty behavior.

We conduct two simulations for read operation with BL_i open. Fig. 8(a) presents the results when the neighbors BL_{i-1} and BL_{i+1} drive BL_i and $\overline{BL_i}$ with opposite logic values (one is logic '1' while the other is logic '0'). The logic value of BL_i remains the same with varying coupling capacitance. This is because the voltage difference between BL_i and $\overline{BL_i}$ is amplified by the sensing circuit, charging BL_i and $\overline{BL_i}$ to opposite logic values. The output of the open bitline is reinforced by both of its neighboring bitlines. We denote this faulty behavior as *compatible coupling* fault.

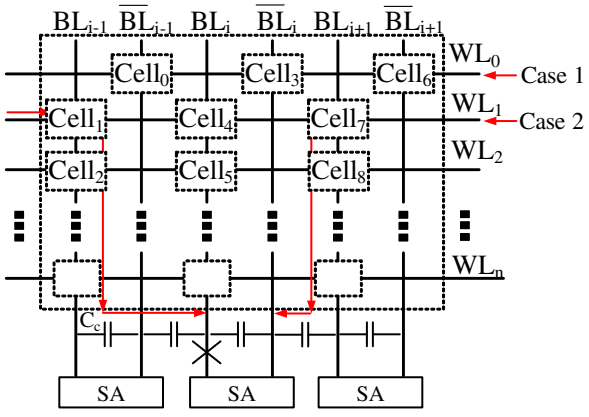


Figure 7. Read with Bitline Open: An Example.

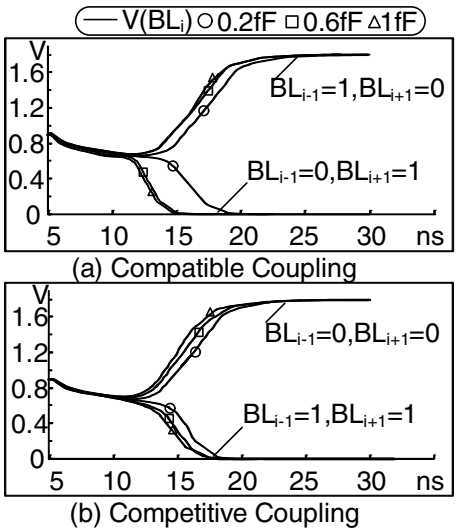


Figure 8. Compatible and Competitive Coupling in Read Operation with BL_i Open.

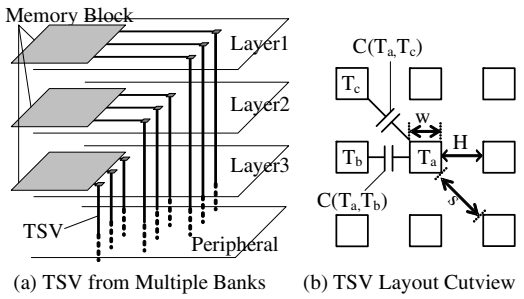
Fig. 8(b) presents the results when two neighbors, BL_{i-1} and BL_{i+1} drive BL_i and $\overline{BL_i}$ with the same logic value (both '1' or both '0'). Simulation results show that the logic value of open bitline BL_i is determined by $Cell_7$, since $Cell_7$ is coupled with $\overline{BL_i}$, the complemental bitline of BL_i. We denote the *driving force* as the capability to drive the open bitline through capacitive coupling. The larger distance between the aggressor bitline (TSVs) and the open bitline (TSV) is, the smaller coupling capacitance is. Since BL_{i-1} and BL_{i+1} have the same storage-cell value during the read operation, they pull up (or pull down) BL_i and $\overline{BL_i}$ at the same time. The coupling capacitance from BL_{i+1} to $\overline{BL_i}$ is larger than that from BL_{i-1} to BL_i, and hence the driving force of BL_{i+1} is larger, making BL_{i+1} dominate the logic value in BL_i. We denote this faulty behavior as a *competitive coupling* fault.

Similar results are obtained with varying coupling capacitance C_c. The reason is that, the sense amplifiers are active during sensing phase of read operation. Even if the coupling capacitance is small (e.g., $0.2fF$) between neighboring bitlines, the small voltage changes in open bitline generated by this coupling capacitance can be amplified by the sensing circuit.

6 TSV Coupling Effects from Multiple Layers

In this section, we consider capacitive coupling from aggressor TSVs on multiple layers. Using Aggressor-Victim Model [26], we can extend our earlier simulation model for such additional TSV coupling effects.

For wordline open simulation, based on the capacitance extraction model presented in [19], we first calculate the sum of capacitance coupled to all possible neighboring TSVs driven by logic '1' and '0', respectively. Then, we change the value of coupling capacitance parameters (e.g. C_1 is the sum of those capacitances coupling to wordlines driven by



(a) TSV from Multiple Banks (b) TSV Layout Cutview

Figure 9. TSV Coupling from Multiple Layers.

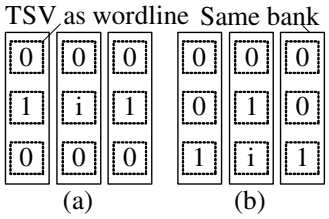


Figure 10. Considering TSV Coupling from Multiple Layers for Wordline Open.

logic '1' and C_0 is the sum of those capacitance coupling to wordline driven by logic '0') with the calculated values and conduct simulation using the same schematic circuit in Fig. 3.

Fig. 10 shows two cases in terms of different wordline access address. 'i' denotes the TSV with open defect while '1' denotes the neighboring TSVs of wordline being accessed. In Fig. 10 (a), the three banks are within the same memory rank so that the wordlines with the same local address within the bank are accessed simultaneously. In many DRAMs, the bank within the same rank can operate independently. Based on this, Fig. 10 (b) shows an extreme case wherein the coupling capacitance from neighboring wordline is maximized. For both cases, the faulty behaviors of write/read operation are similar to previous simulation results (in Fig. 4 and Fig. 5).

For bitline open simulation, the faulty behavior of bitline opens are quite similar to what we have studied in Section 5. We only need to know the driving forces among all the neighbors of the open bitline. If the driving force for logic '1' is larger than that for logic '0', the open bitline read as logic '1' , otherwise logic '0'.

7 Fault Modeling and Test Implications

In this section, we map the TSV open defect into memory functional fault models according to our simulation. The fault models caused by TSV open defect in wordline/bitline are summarized in Table 2. It should be noted that, the no access behavior has been studied in previous works, modeled as stuck-open fault and we can map it into one kind of memory address fault, *AFna* [2].

Open Position	Operation	Mode	Faulty Behavior	Fault Model
wordline with open defect(WL_o)	access WL_o	read/write	no access	AFna
	access neighbor of WL_o	read	multiple access	*RDF*
bitline with open defect (BL_o)	access BL_o and its neighbors	write	no access	AFna
		read	coupling from neighbors	*NPSF*

Table 2. Summary of Fault Models.

Wordline Open:

When we access the wordline with TSV open defects, we cannot access the corresponding cells, denoted as *No Access Behavior*. Consequently, write operation cannot change the values in the storage-cell, and read operation cannot change the voltage of bitline, leaving the bitlines in reference voltage. While this can be mapped into the *AFna* memory address fault in traditional 2D memory circuits, the difference is that, all cells within this wordline are unable to access, and all the bitlines within this block stay in reference voltage. Hence, any capacitive coupling from neighboring blocks or neighboring layers could impact the bitline voltages, leading to different faulty behavior under different 3D memory design.

When we access the storage-cell on the neighboring wordline of the wordline with open defect, the floating cell on this wordline is accessed too, depending on the wordline load capacitance and trapped charges within the gate of pass-transistor deposited during fabrication. This faulty behavior is defined as *Multiple Access Behavior*. For write operation, the floating cell cannot be modified with relatively large load capacitance. For read operation, the logic value in bitline (*BL*) and the content in accessed cell ($Cell_1$) are both incorrect (Fig. 5(a)-(b)), denoted as a *Read Disturb Faults* (*RDF*) [27].

Bitline Open:

The write operation with bitline opens has negligible impact on its accessed cell, denoted as *No Access Behavior*. In this work, we only model the fault of read operation with bitline opens. As discussed in Section 5.3, there are two types of coupling faults caused by bitline with open TSV, denoted as *compatible coupling faults* and *competitive coupling faults*, respectively. Suppose BL_i is open and given the logic values in BL_{i-1} and BL_{i+1}, Table 3 presents the logic value of BL_i caused by capacitive coupling. Once a wordline is selected, all storage-cells in this wordline are accessed. These accessed cells might be in two positions: bitlines (BL_1, BL_2,...,BL_i) or complemental bitlines ($\overline{BL_1}$, $\overline{BL_2}$,...,$\overline{BL_i}$). As mentioned in Section 5.3, compatible coupling faults are sensitized when two neighbors of the bitline with open defect (BL_i) have opposite logic values while competitive coupling faults are sensitized when these two neighbors have the same logic values (see Column 2 and Column 4 for compatible coupling and Column 6 and Column 8 for competitive coupling). Let us take the first row in compatible coupling faults (see Ta-

	Compatible Coupling				Competitive Coupling			
CellPosition	BL_{i-1}	(open)BL_i	BL_{i+1}	Test	BL_{i-1}	(open)BL_i	BL_{i+1}	Test
	1	***1***	0	α	1	***0***	1	γ
In *Bitline*	0	***0***	1	β	0	***1***	0	γ
	1	***0***	0	α	1	***0***	1	γ
In $\overline{Bitline}$	0	***1***	1	β	0	***1***	0	γ

Table 3. Fault Modeling for Read Operation with Bitline Open.

ble 3) as an example. When WL_1 in Fig. 7 is selected, $Cell_1$ and $Cell_7$ are accessed, driving BL_{i-1} and BL_{i+1} to logic '1' and logic '0', respectively. Then, BL_{i-1} drives BL_i to logic '1' and BL_{i+1} drives $\overline{BL_i}$ to logic '0'. The output of BL_i is hence logic '1'.

The faulty behavior in read operation with bitline open defect can be mapped to the well-known neighborhood pattern sensitive fault (NPSF). We develop the following tests to cover all the faulty behavior shown in Table 3:

$$\alpha : \{\Uparrow (w0); \Uparrow (r0, w1, r1)\}$$
$$\beta : \{\Uparrow (w1); \Uparrow (r1, w0, r0)\}$$
$$\gamma : \{\Uparrow (w1); \Uparrow (r1)\}$$

Wordline/Bitline TSV Open with Multi-Layer Coupling:

The crossing bank effect of capacitive coupling changes the normal memory test algorithms dramatically. That is because, in 2D memory, the test in different memory bank are independent, making it possible to test the memory chip in a highly parallel manner. However, in 3D memory, we have to write test patterns to memory cells in multiple banks to satisfy the test condition.

8 Conclusion and Future Work

The large number of TSVs implemented in 3D-stacked DRAM circuits are prone to open defects and coupling noises, leading to new test challenges. In this paper, we model the faulty behaviors of such defects with extensive simulation studies, map them into memory functional fault models, and present the corresponding test implications.

In our future work, we plan to study test algorithms and the associated BIST structure to detect TSV open defects. In addition, this work focuses on TSVs with full open defects. As TSVs can also be resistive open [27] and may exhibit different faulty behavior, we plan to also consider resistive open defect on wordline/bitline in our future work.

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