Design for Manufacturing With Emerging Nanolithography

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***Abstract*—In this paper, we survey key design for manufacturing issues for extreme scaling with emerging nanolithography technologies, including double/multiple patterning lithography, extreme ultraviolet lithography, and electron-beam lithography. These nanolithography and nanopatterning technologies have different manufacturing processes and their unique challenges to very large scale integration (VLSI) physical design, mask synthesis, and so on. It is essential to have close VLSI design and underlying process technology co-optimization to achieve high product quality (power/performance, etc.) and yield while making future scaling cost-effective and worthwhile. Recent results and examples will be discussed to show the enablement and effectiveness of such design and process integration, including lithography model/analysis, mask synthesis, and lithography friendly physical design.**

***Index Terms*—Design for manufacturing, double patterning, e-beam lithography (EBL), EUV lithography (EUVL), multiple patterning, nanolithography, physical design.**

I. Introduction

SHRINKING feature sizes for very large scale integrated circuits (VLSI) with advanced lithography has been a holy grail for the semiconductor industry [1] to achieve ever-higher device density and performance with reduced cost per transistor. This amazing scaling, while posed to continue according to the ITRS roadmap [2], has been facing grand challenges. As shown in Fig. 1(a), the industry has been pushing the limit of the 193-nm wavelength lithography to print features much smaller than the wavelength (e.g., 45 nm, 32 nm, 22 nm), with many innovative technologies, including immersion lithography [3], [4], restrictive design rules [5], extensive and even exotic resolution enhancement techniques (RETs) [6]–[9], and advanced source-mask optimization (SMO) [10]–[12].

It was hoped that the extreme ultraviolet lithography (EUVL), which has a much shorter wavelength of 13.5 nm, could be ready by now to replace the 193-nm lithography, but EUVL has been notoriously delayed [Fig. 1(a)]. There are still tremendous technology challenges for EUVL, most notably the power sources, resists, and defect-free masks. It is still not certain when EUVL will be ready for volume production, considering both technical and economic issues. This has forced the industry to rapidly adopt double patterning lithography (DPL) for 22-nm and 14-nm nodes [13]–[15]. DPL, or the more general multiple patterning lithography (MPL), at the concept level, just repeats the single patterning lithography by using two or more mask/patterning processes to form coarser patterns, which are then combined to form the original finer patterns [Fig. 1(b)]. A major challenge for MPL is the overlay error, due to mask shifting, rotation, and magnification [16], for both interconnects [16] and transistors [17], [18]. MPL requires layout compliance/decomposition, subject to minimum spacing constraints on each mask. Different types of MPL technologies are being developed [14], [15], [19], [20], with different design/process requirements. For example, as shown in Fig. 1(b), Intel demonstrated to use quadruple patterning to print 7-nm feature/spacing in laboratory environment [21]. Meanwhile, next-generation nanolithography technologies, including EUVL, electron beam (direct write) lithography (EBL), directed self-assembly (DSA), and nanoimprint lithography (NIL), are under intensive research and development for 14 nm, 11 nm, 7 nm, and $1\times$ nm for extreme scaling. They have their own challenges, e.g., low throughput for EBL and high defects for DSA and NIL. Novel design and CAD techniques can help mitigate these challenges and make layouts better accommodate the underlying process restrictions.

The goal of this paper is to provide a survey and perspective on key aspects of design for manufacturing (DFM) with these emerging nanolithography technologies. It will be noted that it is impossible to cover all important lithography/DFM issues here due to the page limit. This paper is not intended to be exhaustive, but rather representative and serve as a starting point for further reading. We pick the topics that are of general and recent interests to the electronic design automation community, including the problems, challenges, recent approaches, and research directions.

The rest of this paper will be organized as follows. In Section II, we will discuss the lithography modeling and analysis issues, in particular on the lithography hotspot detection for physical verification and lithography friendly physical design. Section III will discuss modern mask synthesis issues, with focus on layout decompositions for double/multiple patterning lithography. Section IV discusses standard cell layout design issues. Section V discusses lithography-aware routing.

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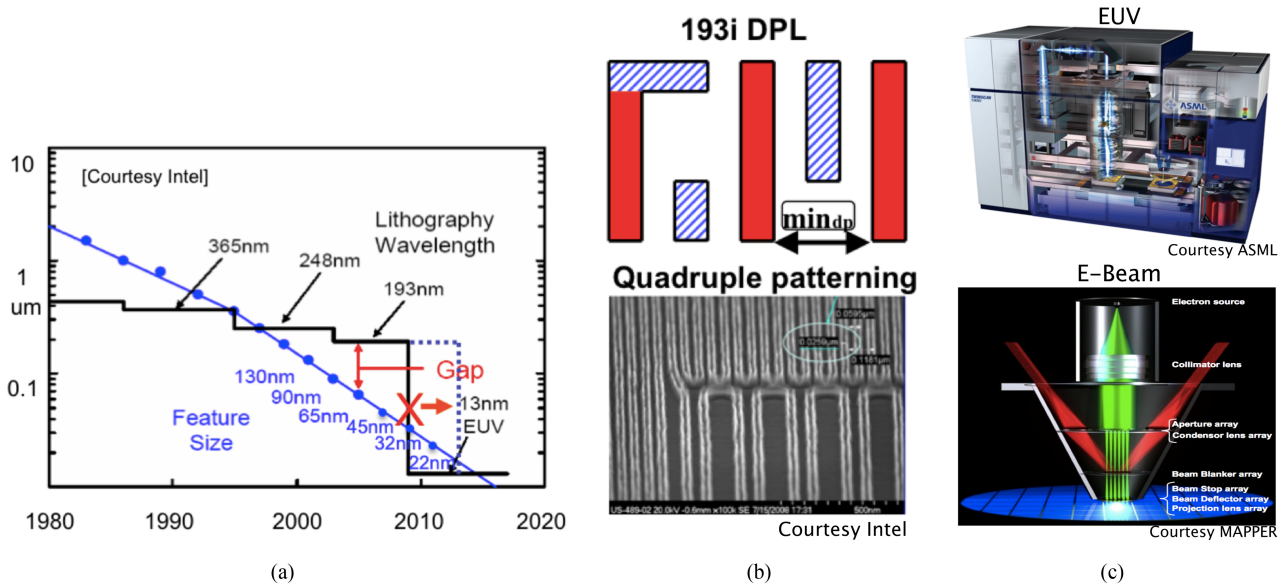


(a) (b) (c)

Fig. 1. (a). The lithography roadmap and EUVL delay. (b) The 193nm extension with double patterning or even quadruple patterning. (c) Other next-generation nanolithography technologies such as EUVL and EBL.

Sections VI and VII will discuss emerging EUV and e-beam lithography related CAD issues, followed by the conclusion in Section VIII.

II. Lithography Modeling and Analysis

With continuous shrinking of semiconductor process technology nodes, the minimum feature size of modern IC is much smaller than the lithographic wavelength [2]. One of the greatest challenges is that what one sees at the physical layout stage is not necessarily what one will get after the chip is fabricated. These printability challenges not only cause possible open/shorts, but also lead to parametric yield loss. In the following, we will briefly discuss lithography modeling basics. The detailed topic by itself is beyond the scope of this paper. Interested readers can refer to [22] and [23].

A. Lithography Modeling and Analysis Basics

The fundamental resolution limit of a lithography system can be written as the following Raleigh's equation:

$$R = k_1 \frac{\lambda}{\text{NA}} \tag{1}$$

where R is the minimum resolution (half-pitch), NA is the numerical aperture, λ is the wavelength of the light source (i.e., 193 nm for current mainstream lithography) and k_1 is a coefficient that encapsulates process-related factors. The minimum feature size can be reduced by decreasing this coefficient through computational lithography such as optical proximity correction. However, the theoretical lower bound of k_1 is 0.25.

The depth of focus (DOF) indicates the range of the focus variation in which the printed pattern is robust, which can be estimated as

$$\text{DOF} = k_2 \frac{\lambda}{\text{NA}^2} \tag{2}$$

where k_2 is also a pattern and lithography system dependent factor. To print with smaller resolution at a given wavelength λ, NA has to be increased, which would degrade DOF. Hence, the requirement of controlling process variations becomes tighter. The adoption of immersion lithography can raise the NA to be around 1.35. Therefore, the practical limit of half-pitch for single exposure 193-nm lithography is about 40 nm. Double or multiple patterning lithography has to be used for higher density.

The modeling of the lithography process is extremely complicated. We will only cover some basics. It can be roughly modeled as optical/aerial image generation and patterning/development: 1) the mask shapes are first projected into the photoresist as an aerial image, and 2) the photoresist is developed and patterned based on the image intensity. The aerial image can be modeled by the Hopkins equation, which is a 4-D integral. However, this formulation is too slow to simulate across the full chip. To speed up simulations, the kernel decomposition method can be used [24], and the light intensity at any given location can be written as

$$I = \sum_{n=0}^{p-1} \sigma_n |F \times K_n|^2 \tag{3}$$

where p is the number of kernels to be used (in general, 5 to 10 is good enough), F is the mask transmission function, σ_n's and K_n's are the set of constants and functions that are derived from the optical system. The convolutions can be retrieved by looking up the precomputed convolution values [24].

Once the aerial image is obtained, it will guide the photoresist development and etching. Such modeling is very complicated due to complex physics and chemistry processes, which is beyond the scope of this paper, and interested readers can refer to [25] for details. However, to the first order, simple or variable threshold models can be used to determine the printed contour [24]. The contour location $\boldsymbol{x}$ is taken such that

the image intensity equals some intensity threshold depending on some image characteristics (denoted as a dot) in

$$I(\boldsymbol{x}) = I_{\text{th}}(\cdot). \tag{4}$$

It will be noted that even state-of-the-art semiconductor manufacturing still suffers process variations, e.g., dosage, focus, and so on. It is important to model the printed images under process variations. Doing it naively with extensively process window sampling will be prohibitively expensive. In [26], a variational lithography model method was proposed, based on the kernel decomposition and variational edge placement error computation. The process variations can be modeled through two basic effective variations in dosage and focus. From this, the variational printed image can be obtained, under process-variation (PV) band [27].

The line edge roughness (LER) in the past was a second-order variation, as the critical dimension was much larger than LER. However, LER does not scale as feature size gets smaller, thus LER has become an increasingly larger fraction of the critical dimension (CD) variation. The main factors for LER include erosion of polymer aggregates at the edge of photo-resist during the etching/development process, and shot noise effect for EUVL and EBL. LER can be modeled as a power spectral density (PSD) function [28]. While LER is mostly believed a random effect, it indeed displays layout-dependent variations as LER depends on the aerial image quality. Higher aerial image contrast results in a smaller transition region in photo-resist polymer dissolution that reduces LER. In [29], the image log-slope is added to LER modeling to consider proximity effects such as pitch spacing for a 32-nm process with 193-nm lithography. A layout-dependent LER model for PSD can be written as follows:

$$S(f) = \frac{2\sigma(x)^2 L_c}{(1+k^2 L_c^2)^{0.5+\alpha}} \tag{5}$$

where the RMS roughness $\sigma(x)$ models the layout proximity effects such as pitch. The parameter L_c is the correlation length, and α is related to the edge smoothness. With the new layout-dependent power spectral function $S(f)$, line edge roughness can be reconstructed by applying a random phase to each frequency component of PSD and performing inverse Fourier transform [30]. LER will be a limiting factor for nano-lithography processes including EUVL and e-beam lithography. New modeling techniques for LER will be needed to consider different proximity effects for emerging lithographies.

Once the geometrical shape is obtained for a given layout, we can model its electrical behavior, e.g., timing, power. For non-rectangular gates, the slicing technique has been widely used for gate delay and leakage analysis (Fig. 2) [31]–[33]. It will be noted that timing and leakage behave very differently when the gate length changes; thus, the equivalent gate lengths for timing and leakage will be different for nonrectangular gates.

B. Lithography Hotspot Detection

In order to bridge the wide gap between design requirements and manufacturing limitations of the current mainstream 193-nm lithography, various DFM techniques have been proposed to improve product yield and avoid potentially problematic patterns (i.e., process hotspots). However, even with these RET, for very deep subwavelength processes, lithography hotspots still exist even after applying these DFM techniques. Fig. 3 shows the printed images of two local regions from certain 32-nm design after applying RETs. We can see that there are various types of process hotspots, featuring complex patterns related to line-ends, jogs, corners, contacts, etc.

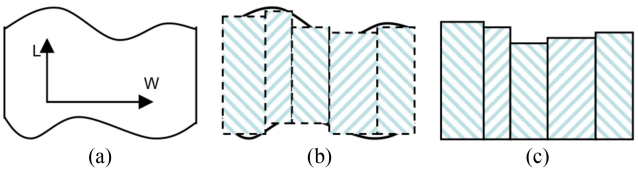


Fig. 2. Nonrectangular gate and slicing for electrical analysis [33]. (a) Nonrectangular gate after printing. (b) Gate is sliced into small pieces along the channel. (c) Each slice will be modeled by its equivalent gate length. They will be combined to get the equivalent gate length for the original gate.

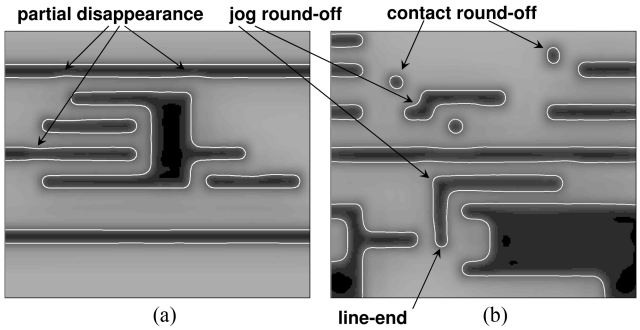


Fig. 3. (a) and (b). Two examples of lithography hotspot patterns [36].

Detailed computational lithography simulations [34], [35] have been used to obtain accurate pattern images, but they are extremely computational intensive, and thus may not be suitable for detecting these hotspots on a full-chip scale while having fast turn-around-time to guide early IC physical design. To raise the level of abstraction for efficient physical verification and physical design, it is often needed to know that for a given layout, whether there is any lithography hotspot (i.e., poor printability) and where quickly.

The goal of the hotspot detection problem is to identify all hotspot locations in the layout without running CPU-intensive lithography simulations. The main challenges are how patterns are represented and how they can be matched in the full layout. In recent years, several representations and hotspot detection algorithms have been proposed. They can be categorized into two mainstreams: pattern matching and machine/data learning, which will be discussed as follows.

1) *Pattern Matching Based Hotspot Detection:* In pattern matching based approaches, a hotspot pattern is described by an explicit model, and the detection process is to match the model with all layout patterns. These approaches are usually more accurate and faster than machine learning based approaches, but they rely on a set of predefined hotspot patterns.

Kahng *et al.* [37] presented an early work to build a graph for the full layout to reflect pattern-related CD variation. The edge weight models the CD variation and hotspots can be

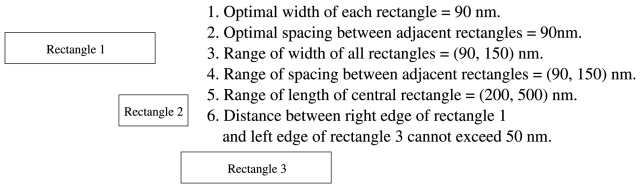


Fig. 4. Example of range pattern staircase [39].

determined according to an user-specified threshold value. The CD variation is evaluated based on corner-induced variations that may lead to corner rounding, and proximity-induced variations that may lead to shortening or bridging. However, the CD variation evaluation method is limited and thus this approach generate false alarms.

The concept of range pattern [38] is proposed to incorporate process-dependent specifications, and is enhanced in [39] to represent new types of hotspots. A range pattern is a 2-D layout of rectangles with additional specifications and is encoded by strings. Fig. 4 shows an example of range pattern Staircase. Each range pattern is associated with a scoring mechanism to reflect the problem regions according to yield impact. The hotspot patterns are stored in a predefined library and the detection process performs string matching to find hotspots. This approach is accurate, but the construction of range patterns relies on a grid-based layout matrix, and may be time consuming when the number of grids is large.

Yu *et al.* [40] proposed a DRC-based hotspot detection by extracting critical topological features and modeling them as design rules. These rules are fed to the DRC engine to obtain DRC reports, and then a two-stage filtering process is applied to identify hotspot locations. How to extract critical design rules is a crucial process for the performance because extracting too many rules will lead to numerous false-alarm locations reported by DRC, while extracting too few rules may lead to missed real hotspot locations. This approach is accurate and efficient, but design rules need to be extended to consider more types of hotspot patterns.

Recently, a fuzzy matching model has been proposed in [41] which can dynamically tune appropriate fuzzy regions around known hotspots. This approach utilizes density-based encoding, and iteratively grow fuzzy regions to train the matching model.

2) *Machine Learning Based Hotspot Detection:* The machine learning based approach can naturally deal with unseen patterns. In the machine learning based methods, the regression model is built from a set of training hotspot patterns, and then the regression models are used to predict or detect the hotspots. A good set of training patterns is very important for the successful application of these regression models for hotspot detection. A neural network judgment based detection flow was proposed in [42], where 2-D hotspot image patterns are directly used to train an artificial neural network (ANN) kernel. In [43], a support vector machine (SVM)-based hotspot detection method is utilized through performing 2-D distance transform and histogram extraction on pixel-based layout images. In [44] and [45], SVM is employed for hotspot detection through extraction and classification of certain special layout density-related metrics. Ding *et al.* [46] proposed a high performance hotspot detection methodology with successive performance refinements, where both ANN and SVM are applied. Recently, in [36], a hotspot detection flow was proposed to hybridize the strengths of machine learning models and pattern matching models. Such a flow feeds data samples to a pattern matcher first, and then employs machine learning classifiers to further examine the nonhotspot data set produced by the pattern matcher.

To take advantage of all techniques discussed above, and to achieve a better hotspot detection accuracy, metadetector could be a good choice. The classical flow for one metadetector is illustrated in Fig. 5. This consists of two steps, the calibration and the detection phases. In the calibration stage, the base classifiers and the weighting functions are configured and optimized using training data sets. Here, base classifiers can be any individual hotspot classifiers that are optimized under certain performance metric, including pattern matching and machine learning classifiers, and metaclassfier can be formulated and optimized via proper combinations of multiple base classifiers under a set of weighting functions to further enhance hotspot prediction performance. Phase2 is the stage when the established metaclassifier is applied onto new testing data sets. This stage can operate at very high speed without accurate lithography simulations. How to construct the metaclassifier is the core of the whole flow. For every layout pattern geometry, certain key hotspot features are extracted and then fed into each base classifier. The final metadecision is the weighed sum of base classifiers. Ding *et al.* [36] showed that the optimization of the weighting functions given certain calibration data can be formulated into a quadratic programming, which can be solved optimally in polynomial time.

Fig. 6 compares the performances of four methodologies, EPIC (a metadetector in [36]), ANN, SVM, and pattern matching based method. Here, hotspot accuracy is the rate of correctly predicted hotspots among the set of actual hotspots, and hotspot false-alarm is the rate of incorrectly predicted nonhotspots over the set of actual hotspots. We observe that EPIC (metadetector), in general, shows higher hotspot accuracy as well as lower false-alarm. We also see that pattern matching methods are not good at detecting new types of hotspots without obvious penalty in hotspot false-alarm. In this sense, machine learning can make pattern matching more robust to predict new/unknown hotspots, especially when pattern enumeration becomes costly.

3) *Clustering in Hotspot Detection:* Since the layout hotspots are already the DRC clean layout patterns, the number of nonhotspot patterns greatly outnumbers the total number of hotspot features in the layout [47]. For example, there are hundreds of millions of patterns for each mm^2 layout, but the number of hotspots may be only less than 100. The imbalance between hotspot and nonhotspot data is called imbalanced populations. Since traditional hotspot detection methods rely on having similarly weighed populations, it is important to overcome the imbalanced population problem. Besides, the training data involve a huge number of information, to avoid long runtime penalty, clustering could be helpful to

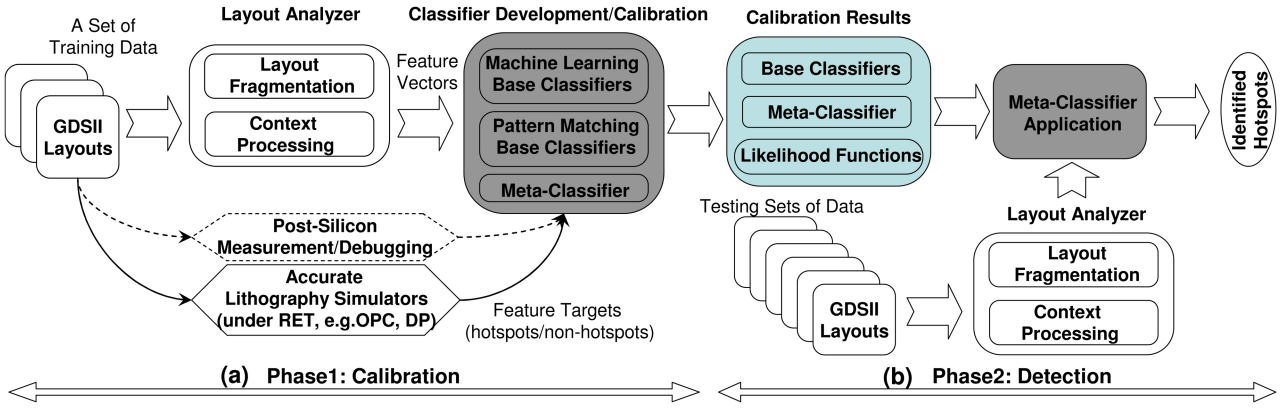


Fig. 5. Overall CAD flow proposed in [36] for hotspot detection based on metadetection formulation.

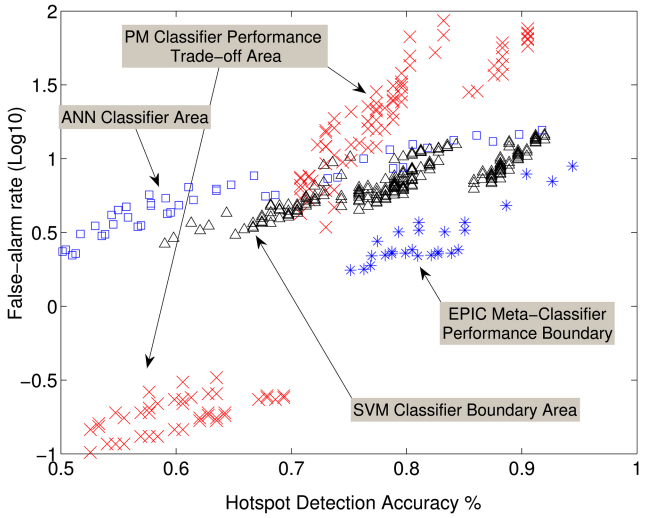


Fig. 6. Tradeoff between hotspot accuracy and false-alarm using various pattern matching and machine learning methods [36].

reduce some data redundancy. In [48] and [49], the extracted hotspots are classified into clusters by data mining methods. The representative hotspot in each cluster is then identified and stored in a hotspot library for future hotspot detection. Guo *et al.* [50] further extended the previous works using improved tangent space based metric.

The lithography hotspot detection has received much research interest in both academia and industry. Recently, the 2012 International Conference on Computer Aided Design (ICCAD) ran a CAD contest on "Fuzzy Pattern Matching for Physical Verification." A set of benchmarks were released by Mentor Graphics, a leading company in DFM to boost academic research and advance the state-of-the-art [47]. The problem and benchmarks are very challenging. The best academic solutions still have a big room for improvement. We expect that more research advancement will be made due to the release of more industry benchmarks. How to take advantage of clustering meanwhile avoid the performance degradation is an open question.

III. Mask Synthesis

Mask synthesis is a key step that has been conventionally performed at the fab. Essentially, when the design is sent to a fab for manufacturing, the fab has to massage the layout so that it can be printed with high fidelity and yield, using various RETs. In this section, we will first give a brief overview of the current status of the single exposure resolution enhancement techniques, in particular, optical proximity correction that is pervasively used. The usage of optical proximity correction (OPC) essentially reduces the k_1 factor in Raleigh's equation. However, no matter how well an OPC is, the theoretical limit of k_1 is 0.25 and the half-pitch limit of single exposure lithography is around 40 nm with 193-nm lithography. To scale further with the 193-nm lithography for 22 nm, 14 nm and beyond, one has to use double or even multiple patterning, where a fundamental problem is how to decompose the original layout into two or more masks, which will be the focus of this section.

A. Resolution Enhancement Techniques

Resolution enhancement techniques are the tricks that lithographers make such that the final printed shapes resemble the drawn ones. The commonly used RETs include OPC, phase-shift mask (PSM), and off-axis illumination (OAI). Since the light intensity distribution strongly depends on the layout proximity, OPC essentially tweaks the layout to compensate the adverse effects, e.g., by line end extension, scattering bar and subresolution assist feature insertion, and so on. PSM and OAI manipulate the light phase and source, respectively, to achieve high-contrast printed images.

Modern OPC engines have to rely on accurate lithography simulations/models, and some attempts have been made to incorporate the process window awareness [26], [51], [52]. Due to process variations, OPC needs to be variation aware to cover different process windows. However, doing it with straightforward process window sampling could be ineffective and prohibitively expensive. In [26], an efficient process-variation-aware OPC (PV-OPC) framework was proposed, which is enabled by an analytical variational lithography modeling. PV-OPC takes only about 2–3 $\times$ runtime compared to previous OPC that assumes a nominal process condition, yet PV-OPC explicitly considers the two main sources of process variations (dosage and focus); thus, it is much more robust.

While most OPC algorithms are based on edge segmentation and movement, the entire mask can also be pixelated.

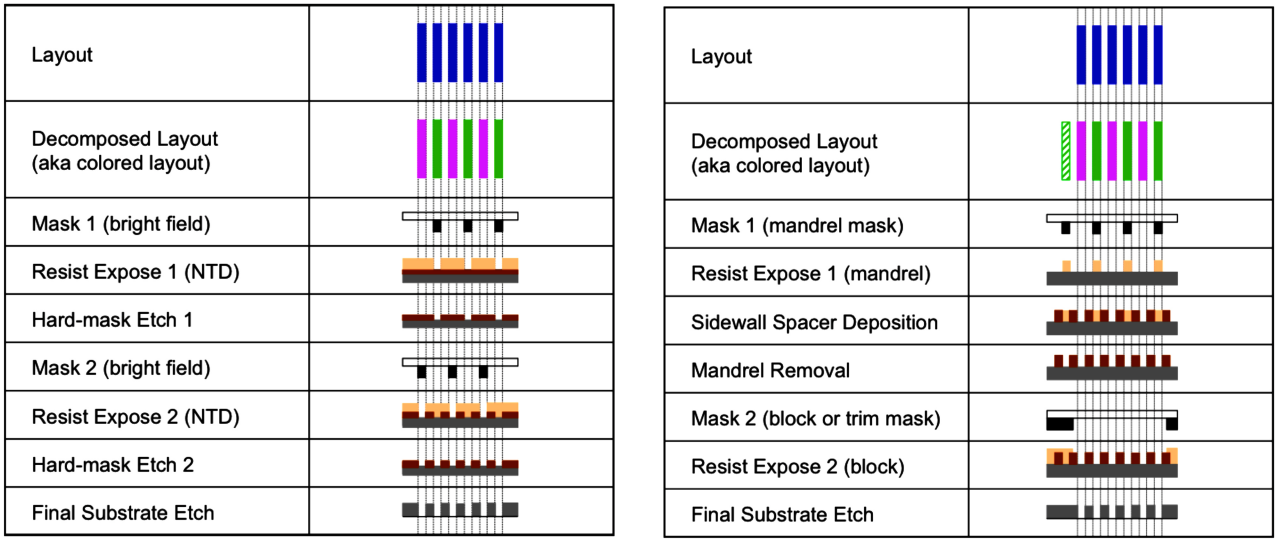


Fig. 7. Manufacturing processes of the two main double patterning lithography technologies. (a) LELE. (b) SADP. (Courtesy of IBM.)

The problem then becomes an inverse lithography and pixel flipping problem [53]. Still, as the inverse lithography is not a one-to-one mapping problem, one has to pick a right objective function, e.g., to reduce the mask complexity while trying to get an acceptable edge placement error [54]. Recently, there is much research interest to perform the SMO, which essentially combines the generalized OAI and OPC together to push the envelope of resolution enhancement with single exposure lithography [12].

It will be noted that while the main and conventional goal of RET is to preserve the layout to fabrication fidelity, there are also studies on electrical OPC, which attempt to meet the design intent for timing and power while reducing the OPC complexity [55]–[58]. Such tighter design intent and process integration plays a more and more important role in design and technology co-optimization.

B. Layout Decomposition for DPL/MPL

DPL has been considered the most viable option for 22-nm/14-nm technology nodes. The advantage of DPL is that the effective pitch can be double, which improves the lithography resolution. There are two main types of DPL with different design/process requirements: litho-etch-litho-etch (LELE) and self-aligned double patterning (SADP). As illustrated in Fig. 7, LELE uses two lithography exposures and etches on hard-mask to create smaller chip features. SADP works by depositing a spacer layer over the chip covering all hard mask features. The covered layer is selectively etched away leaving two sidewalls along any ridge, and then the ridge is removed. Both LELE and SADP can be naturally extended for MPL, which can further improve the resolution. At the concept level, MPL just repeats the single patterning lithography by using two or more mask/patterning processes individually to form coarser patterns and then combines them to form finer pitches.

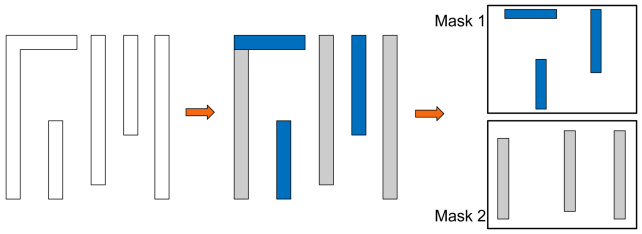
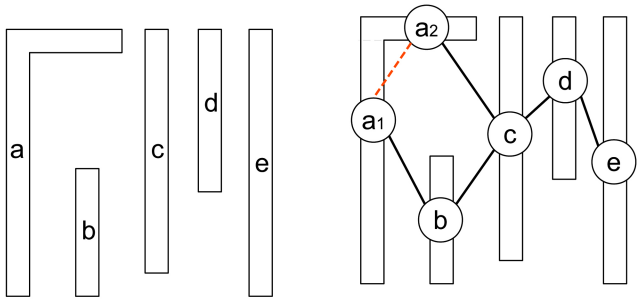


Fig. 8. Example of LELE layout decomposition.

Layout decomposition is a fundamental problem for DPL/MPL that decomposes the original layout into two or multiple masks. In the following, we will survey recent DPL layout decomposition work, followed by some MPL layout decomposition. It will be noted that the impact of DPL/MPL involves in other design steps, e.g., standard cell design, placement, and routing. Issues in standard cell design and placement will be discussed in Section IV, while the DPL/MPL-aware routing will be introduced in Section V.

1) *Layout Decomposition for LELE:* In the LELE layout decomposition, the original design is split into two masks when the distance between two patterns is less than minimum colorable distance; otherwise, coloring conflict occurs. An example of LELE layout decomposition is shown in Fig. 8, where different masks are represented by different colors. Note that the coloring conflict can be also resolved by inserting stitches to split a pattern into two touching parts. However, stitches lead to yield loss due to overlay errors [59]. Therefore, two of the main objectives in LELE layout decomposition are conflict minimization and stitch minimization.

The layout decomposition can be carried out on graph representations. Given an input layout [Fig. 9(a)], after some preprocessing, conflict graph is constructed, as shown in Fig. 9(b). The conflict graph is an undirected graph with a set of vertices V that represent the set of features of input layout, and two sets of edges, conflict edges (CE) and stitch



(a) (b)

Fig. 9. (a) Given input layout. (b) Constructed conflict graph, where one stitch edge is introduced.

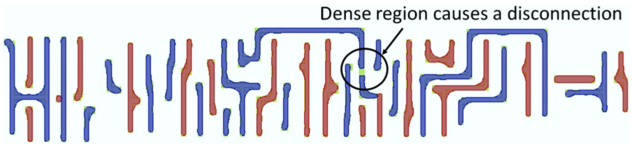
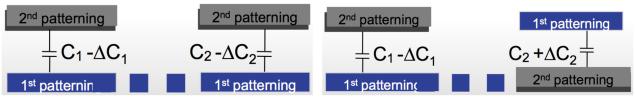


Fig. 10. Unbalanced decomposition may have a patterning problem [67].



(a) (b)

Fig. 11. (a) Layout decomposition without considering overlay compensation. (b) Layout decomposition considering overlay compensation [67].

edges (SE). An edge is in CE if and only if two disconnected features are within the minimum coloring distance min_s of each other. An edge is in SE if and only if two connected features can be assigned to different colors. For example, in Fig. 9(b), the solid edges are the conflict edges, while the dashed edges are the stitch edges and function as stitch candidates. Note that sometimes stitch is not allowed in layout decomposition; then, layout graph and decomposition graph are the same.

To simultaneously minimize the conflict and stitch numbers, the generic mathematical formulation of layout decomposition can be written as follows:

$$\min \quad \sum_{e_{ij} \in CE} c_{ij} + \alpha \sum_{e_{ij} \in SE} s_{ij} \tag{6}$$

$$\text{s.t.} \quad c_{ij} = (x_i == x_j) \qquad \forall e_{ij} \in CE \tag{6a}$$

$$s_{ij} = x_i \oplus x_j \qquad \forall e_{ij} \in SE \tag{6b}$$

$$x_i \in \{0, 1\} \qquad \forall i \in V \tag{6c}$$

where α is a user-defined parameter to represent the relative importance of stitch insertion penalty. It will be noted that for back-end-of-line (BEOL) layer parasitic impact of overlay error or stitch may be negligible [60]; therefore, the α value can be modified accordingly for different layers. For each rectangle r_i, x_i is used to represent its color. c_{ij} is a binary variable for conflict edge $e_{ij} \in CE$ and s_{ij} is a binary variable for stitch edge $e_{ij} \in SE$. Constraint (6a) is used to evaluate the conflict number when touch vertices r_i and r_j are assigned different colors (masks). Constraint (6b) is used to calculate the stitch number. If vertices r_i and r_j are assigned the same color (mask), stitch s_{ij} is introduced.

Formula (6) has been implemented through integer linear programming (ILP), with some variations [61], [62]. However, the ILP-based method suffers from long runtime penalty since it is well-known NP-hard. To achieve speedup, several graph-based methods, i.e., independent component computation, and bridge computation and removal, can be proposed without sacrificing the solution quality. In addition, a matching-based decomposer is proposed to heuristically minimize both the conflict and stitch numbers [63]. This method can only be adopted on the planar layout graph, but in DPL the layout graph may not be planar under the Euclidean distance metric [64], [65].

Instead of minimizing stitch and conflict at the same time, another strategy is to remove conflicts first and then minimize the stitches. In other words, the layout decomposition incorporates two stages. In the first stage, odd-cycle detection is applied to identify and remove the conflicts, while in the second stage the stitch number is minimized. Although this two-stage strategy cannot guarantee a minimal conflict number, it can be solved effectively. Xu *et al.* [66] introduced a flipping graph, which clusters the vertices into several groups and different groups are only connected by stitch edges. Then, a cut-based approach is adopted to the flipping graph to minimize the stitch number. The flipping graph introduced can effectively reduce the problem size. Tang *et al.* [65] introduced a graph, called stitch graph, to represent all stitch candidates. They showed that the stitch graph is plannar, and the stitch minimization problem can be transferred into a min-cut problem, which can be optimally solved in polynomial time.

Unbalanced density may cause lithography hotspot as well as lowered CD uniformity due the irregular pitch, and one example of such a patterning problem is shown in Fig. 10. Furthermore, in LELE double patterning, overlay is a serious concern. To mitigate the overlay induced timing impact, one may try to interleave the coloring such that the timing variations can be cancelled out. For example, in Fig. 11(a), the lower net is assigned to the blue mask while the upper net is assigned to the gray mask. The overlay error due to shifting between the two masks will change the wire spacing between these two nets, which will cause coupling capacitance and timing variations. However, with an overlay-aware layout decomposition scheme as shown in Fig. 11(b), the net effects of ΔC_1 and ΔC_2 due to overlay always compensate each other. Therefore, the ultimate timing variation can be significantly mitigated. Yang *et al.* [67] proposed a systematic, min-cut based, multiobjective layout decomposition framework that can simultaneously consider stitch number minimization, density balancing, and overlay compensation.

It will be noted that in DPL, even with stitch insertion, there may be native conflicts. To resolve these native conflicts, several works introduce layout modification to further minimize the conflict number. Hsu *et al.* [68] proposed a simultaneous layout migration and decomposition for standard cell design.

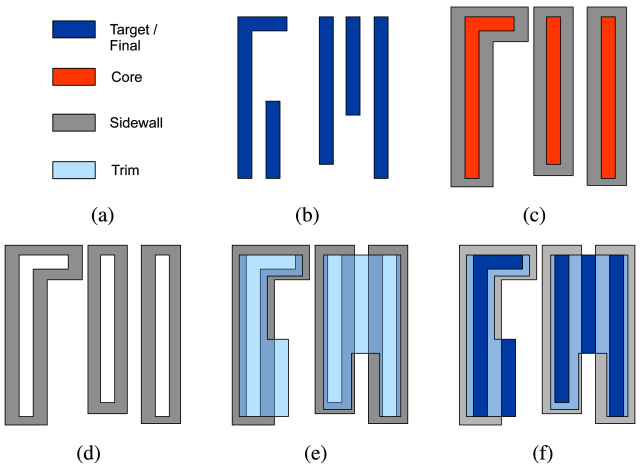


Fig. 12. SADP process of generating some sample 2-D layout. (a) Some labels. (b) Target features. (c) Core patterns and spacers generation. (d) Spacers after core patterns removal. (e) Trim mask. (f) Final patterns.

Yuan *et al.* [69] provided an integer linear programming to obtain as little layout perturbation as possible. Fang *et al.* [70] presented a native conflict prediction method based on the geometric relation of features and a feature perturbation algorithm to minimize native conflicts. Ghaida *et al.* [71] formulated the problem of conflict removal as a linear program (LP). However, layout modification may cause new problems, i.e., timing closure and new lithography hotspot. How to integrate timing closure and hotspot avoidance during layout decomposition and modification is still an open problem.

2) *Layout Decomposition for SADP:* Fig. 12 shows a typical spacer-is-dielectric (SID) process of generating some 2-D BEOL layouts. To generate the target features in Fig. 12(b), core mask is first used to generate the core patterns. Sidewall spacers are then deposited around the sides of the core patterns. These steps are illustrated in Fig. 12(c), where the orange rectangular shapes are core patterns generated by core mask, while the grey shapes are sidewall spacers deposited adjacent to the corresponding core patterns. Then, the core patterns are removed, as shown in Fig. 12(d). Finally, trim mask is applied to trim out the desired region [Fig. 12(d)]. Note that only the area that is covered by trim patterns but not covered by sidewalls will be etched. Fig. 12 shows one example of implementing the given target layout. Usually, there may be alternate layout decomposition solutions, and the overlay error is often the main concern when deciding how to assign patterns to masks. Compared with LELE, SADP needs more processing steps. However, the sidewall spacers provide a margin to tolerate the overlay error caused by the unexpected misalignment of two masks. Essentially, if the edges of a nonmandrel pattern (pattern that is not defined by the mandrel mask) is aligned to spacers, the edges will not be affected by the overlay error, which also implies no CD variation for this particular pattern. Therefore, by carefully designing the mandrel and the trim mask, SADP can be less vulnerable to or even avoid the CD variation caused by the overlay error.

Since SADP does not allow any stitch insertion and its width/spacing is more restrictive, it puts more constraints for layout patterns. For example, the layout patterns in Fig. 8 need

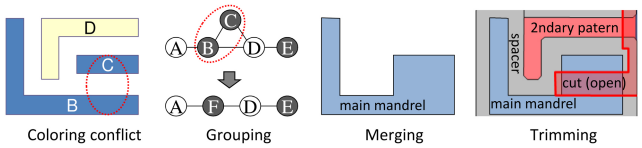


Fig. 13. Grouping and merging coloring for spacer-based multiple patterning [74].

to be modified to be decomposed through SADP. Besides, the trim mask patterns will also be very different from the original layouts. All of these make SADP layout decomposition more complicated and less intuitive, especially for the 2-D layout patterns.

Similar to that in LELE, the layout decomposition of SADP can be formulated as ILP [72], [73]. In ILP formulation, several other issues, e.g., lithography hotspot, can be integrated into the objective function. However, the ILP based method may suffer from long runtime. Ban *et al.* [74] proposed a graph-based flow for SADP layout decomposition. As illustrated in Fig. 13, the problem is formulated as a two-coloring problem, where the patterns are either fabricated by the mandrel mask with the blue color, or through the trim mask with the red color. Note that sometimes for 2-D layouts, there are inherent conflicts such as patterns *B* and *C*. To address this issue, some ingenuity is needed to merge the original core masks, and later on trim out unwanted patterns. Because the cutting technique introduces extra overlay risk that should be minimized, [74] applies a graph-based approach to find the min-cost merging candidate as shown in Fig. 13. Once the patterns are conflict-free, two-coloring techniques can be applied for the layout decomposition and the extra patterns for merging will be trimmed out using the trim mask. Recently, Xiao *et al.* [75] proposed a new graph formulation for SADP decomposition and showed that two-colorability in the graph is necessary for an overlay-free SADP decomposition solution. This approach is based on 2SAT and thus can be done in polynomial time. In addition, the approach guarantees that a valid solution can be obtained if one exists.

The overlay error can still happen at the trim mask, though not as severe as LELE. Therefore, it is still an urgent requirement to consider the overlapping avoidance and hotspot detection in an effective layout decomposition framework.

Recently, hybrid lithography has been proposed, which combines the conventional 193-nm optical lithography together with high-resolution lithography to enable advanced designs [76]. In the process of hybrid lithography, base features are first created by optical lithography or SADP; then, the high-resolution lithography techniques, such as EUVL and EBL, are applied to cut unwanted areas. Hybrid lithography can achieve better image quality, but increase the manufacturing cost. Determining how features are generated by the combined lithography plays an important role. There have been some studies [77]–[79] on hybrid lithography with SADP and EBL. However, current studies are still limited by 1-D designs, and more general approaches for 2-D layout will be needed.

3) *Layout Decomposition for MPL:* The concepts of LELE and SADP can be extended to MPL, such as

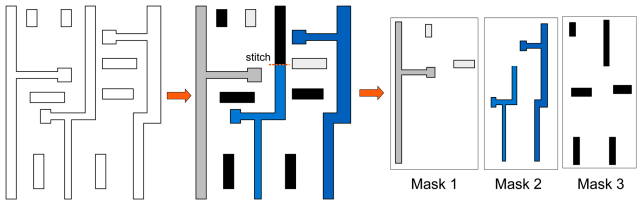


Fig. 14. Layout decomposition for triple patterning lithography (TPL).

LELELE-based triple patterning and self-aligned quadruple patterning (SAQP). At first glance, the layout decomposition for multiple patterning lithography seems easier as there are more masks. However, since the goal of MPL is to achieve finer pitches, there will actually be more features to be packed closer to each other which will form a multiway conflict. In other words, conflict graphs for MPL will become much denser than those in DPL, and they may be nonplanar.

Recently, several papers have extended the LELE decomposition problem to triple patterning lithography (TPL). An example of the layout decomposition is shown in Fig. 14, where the input layout is divided into three colors (masks). Similar to that in DPL, the TPL layout decomposition is carried out on the conflict graphs. Cork *et al.* [80] proposed a simple three coloring algorithm for via array layouts. Yu *et al.* [81] proposed the first TPL layout decomposition methodology for general layouts, where they showed that this problem is NP-hard. Instead of expensive ILP, they proposed a semidefinite programming (SDP) based approximation to achieve tradeoffs between runtime and solution quality. Fang *et al.* [82] presented several graph simplification techniques to reduce the problem size, and a maximum independent set based heuristic method for the layout decomposition. Ghaida *et al.* [83] provided a methodology to reuse the decomposer for DPL, and Kuang and Young [84] proposed a layout clustering method to divide the entire layout into small clusters that can be solved more efficiently.

A very powerful and effective technique for TPL layout decomposition is the graph-based simplification [81], [82]. For example, one technique is called iterative vertex removal, where all vertices with degree less than or equal to two are detected and removed temporarily from the conflict graph. After each vertex removal, we need to update the degrees of other vertices. This removing process will continue until all the vertices are at least degree-three. All the vertices that are temporarily removed are stored in stack S. After solving the color assignment on the remained conflict graphs, the removed vertices are recovered one by one. An example is shown in Fig. 15, where all the vertices can be finally pushed onto stack. Fang *et al.* [82] further proposed a three-edge-connected-component method to partition the original conflict graph into subgraphs.

Instead of ILP formulation or heuristic methods, an SDP-based approximation algorithm was proposed in [81] to achieve good runtime and solution quality. Instead of using a two-bit binary variable to represent three colors, [81] used three unit vectors: $(1, 0), (-\frac{1}{2}, \frac{\sqrt{3}}{2})$ and $(-\frac{1}{2}, -\frac{\sqrt{3}}{2})$ to represent three different masks (Fig. 16). Note that the angle between any two vectors of the same color is 0, while the angle between any two vectors with different colors is $2\pi/3$. The inner product of two m-dimension vectors $\vec{v}_i$ and $\vec{v}_j$ is defined as $\vec{v}_i \cdot \vec{v}_j = \sum_{k=1}^{m} v_{ik} v_{jk}$. Then for any two vectors $\vec{v}_i, \vec{v}_j \in \{(1, 0), (-\frac{1}{2}, \frac{\sqrt{3}}{2}), (-\frac{1}{2}, -\frac{\sqrt{3}}{2})\}$, we have the following property:

$$\vec{v}_i \cdot \vec{v}_j = \begin{cases} 1, & \vec{v}_i = \vec{v}_j \\ -\frac{1}{2}, & \vec{v}_i \neq \vec{v}_j. \end{cases}$$

Based on the novel color representations, the weighted conflict and stitch minimization problem can be written as a vector program (7)

$$\min \sum_{e_{ij} \in CE} \frac{2}{3}(\vec{v}_i \cdot \vec{v}_j + \frac{1}{2}) + \frac{2\alpha}{3} \sum_{e_{ij} \in SE} (1 - \vec{v}_i \cdot \vec{v}_j) \tag{7}$$

$$\text{s.t.} \quad \vec{v}_i \in \{(1, 0), (-\frac{1}{2}, \frac{\sqrt{3}}{2}), (-\frac{1}{2}, -\frac{\sqrt{3}}{2})\}. \tag{7a}$$

Then, the discrete vector program is relaxed to the corresponding continuous formulation, which can be resolved as standard SDP, as shown in (8)

$$\min \sum_{e_{ij} \in CE} \frac{2}{3}(\vec{y}_i \cdot \vec{y}_j + \frac{1}{2}) + \frac{2\alpha}{3} \sum_{e_{ij} \in SE} (1 - \vec{y}_i \cdot \vec{y}_j) \tag{8}$$

$$\text{s.t.} \quad \vec{y}_i \cdot \vec{y}_i = 1, \quad \forall i \in V \tag{8a}$$

$$\vec{y}_i \cdot \vec{y}_j \geq -\frac{1}{2}, \quad \forall e_{ij} \in CE. \tag{8b}$$

From the result matrix Y_{ij}, mapping will be carried out for the three-mask assignment. Essentially, if Y_{ij} is close to 1, nodes i and j should be in the same mask; if Y_{ij} is close to -0.5, nodes i and j tend to be in different masks. The results show that with reasonable threshold such as $0.9 < Y_{ij} \leq 1$ for the same mask, and $-0.5 \leq Y_{ij} < -0.4$ for different masks, more than 80% of nodes/polygons are decided by the global SDP.

Even though two features within minimum space are assigned to different masks, unbalanced density would cause lithography hotspots as well as lowered CD uniformity due to irregular pitches [67], [85], all of these may cause yield loss. Different from DPL where two colors can be more implicitly balanced, due to more colors and the bigger solution space, we need to explicitly consider the density balancing in MPL layout decomposition. However, how to address this issue effectively in MPL is still an open problem.

In terms of self-aligned multiple patterning (SAMP), Chen *et al.* [86] presented a general analysis of technological merits, process complexity and costs of various SAMP techniques. Different techniques show different scaling/resolution capability and process challenges. In addition, each technique has unique CD uniformity and line-width roughness, which affect its application area and the design methodology. Recently, [87] presented a study on manufacturing-friendly design style for SAQP. Performing SAQP layout decomposition for 1-D regular patterns is trivial, however, it is still an open problem to handle 2-D random patterns. Beginning from exploring the feasible feature regions and possible combinations of

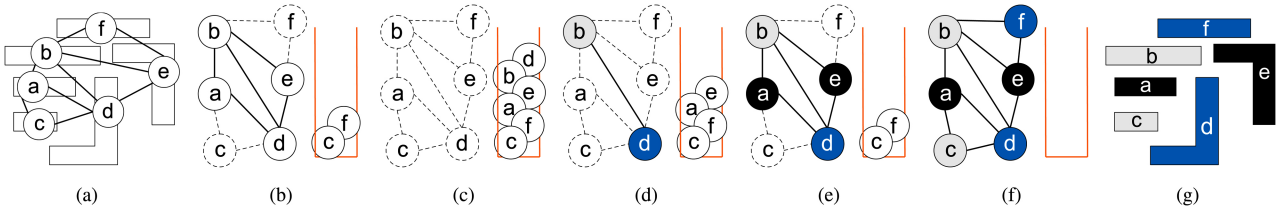


Fig. 15. Iterative vertex removal [81]. (a) Conflict graph. (b) and (c) Iteratively remove and push in vertices with degree no more than two. (d)–(f) After color assignment for the remanent vertices, iteratively pop up and recover vertices, and assign any legal color. (g) Layout decomposition can be finished after the iterative vertex recover.

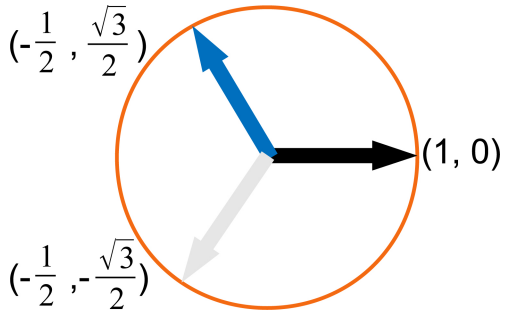


Fig. 16. Vector based color representations.

adjacent features, several geometry rules are defined for SADP friendliness. Based on these rules, an SAQP-friendly layout check and feature region assignment algorithm is presented and are used to analyze common pattern cases.

IV. Lithography Friendly Standard Cell and Placement Issues

Standard cells are fundamental building blocks for modern VLSI circuits. Nanometer standard cells are prone to lithography proximity and process variations. How to design robust cells under variations plays a crucial role in the overall circuit area, performance, power, and yield.

A. Standard Cells

In the past, design rules were simple width/space rules, but as technology scales to 45 nm and below, the number and complexity of design rules explode. Many of these design rules are related to lithography as the optical wavelength has been stuck at 193 nm for multiple generations, while the feature size continues shrinking. The industrial approaches typically apply restricted design rules or identify opportunities in the standard cell layout to enforce as many recommended rules as possible. An example of poly layout restriction from 2-D in 90-nm node to 1-D in 32-nm node is shown in Fig. 17. On the other hand, metal layers, in particular M1, are challenging to strictly follow the unidirectional and uniform pitch routing due to pin access, routing congestion/blockage, and via minimization. It will be noted that variations still exist even with restricted design rules such as single poly direction and pitch due to irregular surrounding patterns, e.g., poly-contact pad to active layer distance, poly end-cap, and so on. Therefore, there is still plenty of room for layout optimization.

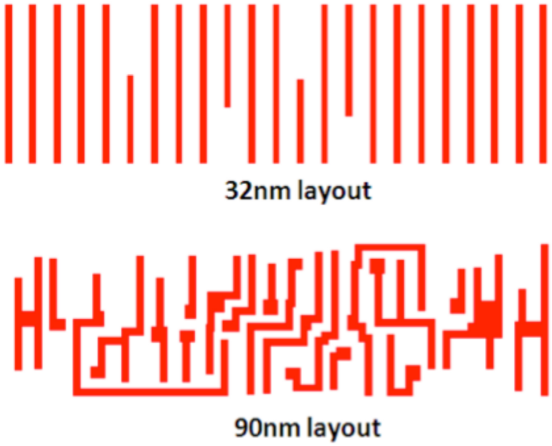


Fig. 17. Poly lines of sample 32-nm and 90-nm layouts (courtesy ARM).

In [88], a total sensitivity based standard cell analysis and layout optimization method is proposed. The total sensitivity includes the transistor criticality, and the lithographic proximity and process variations. The cell layout optimization can be formulated to minimize the cell performance gap. As the gate length continues to shrink with the contact size, the source and drain contact resistance becomes a significant portion of the total on-resistance, which has to be considered during the standard cell layout optimization [89].

With further scaling, there is a trend to move toward more regular fabric or grating [90], by moving the design-to-manufacturing interface from design rules to higher level of abstraction based on a defined set of precharacterized layout templates. Preliminary results have demonstrated that this methodology can simplify optical proximity correction and lithography processes for sub-32-nm technology nodes. These kinds of architectural decisions will play a key role in future IC designs.

B. Placement Composability

The typical optical proximity influence region can span a distance up to five times wavelength, i.e., around 1000 nm for 193-nm lithography. In a 22-nm process, this can cover over ten minimum metal tracks, or standard cell's height. Therefore, a standard cell's printability could be well affected by its neighboring cells, or even nonadjacent cells. That is a serious problem that will affect the placement composability.

To minimize the interference between adjacent cells, dummy poly insertion has been proposed to shield the effects

from neighboring cells [91]. Detailed placement techniques have also been proposed to perturb the layout slightly for better printability [92], [93].

One grand challenge for standard cell and placement under double/multiple patterning lithography is that there may be coloring conflict between adjacent cells. Also, it is still not universally agreed upon whether the cells will be precolored (i.e., during the standard cell layout stage) or post-colored (i.e., flat after standard cell placement of of the entire chip). Actually, the cell characterization itself may depend on its neighborhood and layout decomposition. Thus, it will be very interesting to design new architecture of standard cells together with the coloring schemes to minimize the variations. This is still an open topic.

V. Lithography Friendly Routing

With widening manufacturing gap, even the most advanced resolution enhancement techniques still cannot guarantee what-you-see-is-what-you-get. Increasing cooperation of physical design is a must to generate lithography-friendly layouts. Routing is one of the most important stages in nanometer VLSI physical design, and it is oftentimes challenging lithography problems reside. It is particularly serious in lower metal layers where routing density is very high and wrong way routing is often demanded by designers.

A. General Lithography-Aware Routing

Early lithography-friendly routing studies are investigated and discussed in [94] from post-routing hotspot fixing to during-routing hotspot avoidance guided by various lithography metrics. An extensive survey on manufacturability-aware routing has been presented in [95], where key manufacturability issues including CMP, random defects, and lithographic printability are discussed. More lithography specific studies will be discussed below.

Several works have been proposed to incorporate accurate lithographic models or predictive models into physical design stages, in particular the routing stages, to ensure layout printability. These approaches can be categorized as two types: construct-by-correction and correct-by-construction. Construct-by-correction performs conventional routing first followed by hotspot detection and removal in the post-routing stage; while correct-by-construction integrates a hotspot metric or constrains into the routing engine to optimize the printability during routing.

1) *Construct-by-Correction Approach:* In [24], the concept of lithography hotspot map based on edge placement error (EPE) is proposed to measure the overall printability and manufacturing RET effort. The technique is applied to several RET-aware routing algorithms including EPE guided wire spreading, and rip-up and reroute for post layout optimization. This method requires only one full-chip lithography simulation to filter out EPE hot spots, and thus it achieves fast simulations.

Kong *et al.* [96] proposed a hybrid method to combine a rule-based approach for fast predetection and a model-based approach for post-optimization. Because hotspot detection is computational expensive, rule-based filtering is first applied to select regions for later model-based analysis. The router can then perform correction based on these reduced sets of hotspots with moderate efforts.

Construct-by-correction approaches are straightforward and do not require major redesign of an existing routing engine. However, if there are too many lithography hotspots, its effectiveness will still be limited.

2) *Correct-by-Construction Approach:* OPC-aware maze routing methods are proposed based on multiconstrained shortest path optimization with subgradient method [97] and optical proximity error metrics [98]. In [99], an analytical formula for intensity computation is presented to model post-layout OPC based on a quasi-inverse lithography technique. For each net, the OPC demands of the neighboring free space located in its global routing path are calculated by the quasi-inverse lithography technique. After computing the OPC demand, [99] performed detailed routing considering the wire length and OPC demand to find a real routing path based on the global routing result, where the OPC demand can guide the detailed routing to avoid OPC-prohibited regions. In [100], a compact post-OPC litho-metric for a detailed router is proposed based on statistical characterization. The interferences among weak grids are characterized with one of the predefined litho-prone shapes (e.g., jog-corner, via, line-end). The litho-friendly detailed router is then performed based on this predictive OPC metrics.

To handle general lithography-friendly routing, [101] proposed a hotspot detection technique based on data learning for RETs and integrated it into detailed routing flow. A hotspot detection engine must first have a routing path to provide the routing cost updates. However, during sequential routing, unrouted nets leave blank and uncharacterized regions that lead to an inaccurate hotspot detection. To eliminate uncharacterized regions, [101] proposed a predictive formulas on the top of existing hotspot detection kernels to predict the routing path with the least expected lithographic cost. The data learning applies by a preestablished kernel from a set of sample layouts, and thus helps reduce the runtime overhead during the routing stage.

B. DPL/MPL-Aware Routing

Multiple patterning layout decomposition happens after the physical design has been fixed. Although the goal of robust MPL decomposition is to accommodate as much design intent and process constraints as possible, upstream MPL friendly physical design will be important to obtain more flexibility and better quality of results. There have been recent studies to consider DPL/MPL friendliness during routing in a correct-by-construction manner.

1) *DPL/MPL-Aware Routing for LELE:* A DPL-friendly routing [102] for enhanced decomposability performs detailed routing and layout decomposition simultaneously. Each routing grid is associated with an additional variable that stores its coloring feasibility. While routing a net, the path that introduces fewer DPL-related conflicts will be selected. Redundant via insertion, which is a key yield improvement technique, introduces more complexity in DPL compliance.

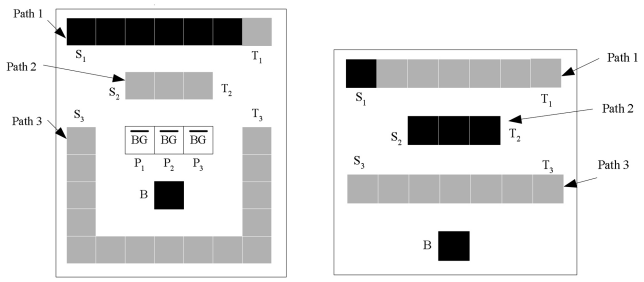


Fig. 18. DPL-aware routing with lazy routing [104]. (a) Coloring together with routing may cause detour. (b) Lazy coloring reduces wirelength.

The challenge comes from the extra metal used to cover the via and the redundant via in both layers. To handle the extra complexity, [103] proposed a detailed routing framework to perform DPL and redundant via co-optimization.

In [104], two techniques, lazy color decision and last conflict segment recording, are proposed to further enhance double patterning friendly routing. The idea of lazy color decision is to delay the coloring of bi-colorable grids until more information is available. Fig. 18 shows an example where a precolored grid B exists and three nets (S_1, T_1), (S_2, T_2), and (S_3, T_3) are to be routed. With a path searching algorithm, $Path1$ is first routed; however, there are several coloring options. If the coloring solution as shown in Fig. 18(a) is selected, $Path2$ and $Path3$ can then be obtained, where a detour is required for $Path3$ to avoid conflict. With lazy coloring shown in Fig. 18(b), the $Path1$ is not immediately colored after its routing, but colored after $Path3$ is obtained. This technique allows more flexibility to reduce the number of stitches and wire length. However, because the coloring is done after the path searching phase, the path searching algorithm may not be able to detect within-path conflicts. To handle this problem, the last conflict segment recording technique is then applied to detect conflicts within a path during routing, which helps improve the success rate of coloring.

Different from DPL where the coloring conflicts can be detected by finding an odd-cycle, detecting TPL or the more general MPL coloring conflict during routing will be much more complicated due to the higher complexity of conflict graph and higher flexibility for color assignment. To solve the maze routing problem for multiple patterning lithography, [105] proposed a unified graph model as shown in Fig. 19. Every vertex in the routing grid is split into 12 vertices in the proposed graph model representing three colors in four routing directions. Fig. 19(a) shows the routes of three nets on the original routing grids, while Fig. 19(b) shows the corresponding routing on the TPL graph model. The shaded regions shown in red and blue are the conflict regions for the red and blue routes, respectively. Routing within a conflict region will induce more cost and, therefore, will be avoided if a conflict-free solution exists. The advantage of this graph model is that it can be easily extended for multiple patterning techniques.

TRIAD [106], a TPL-aware detailed routing based on the LELE process, is proposed to perform gridless routing and

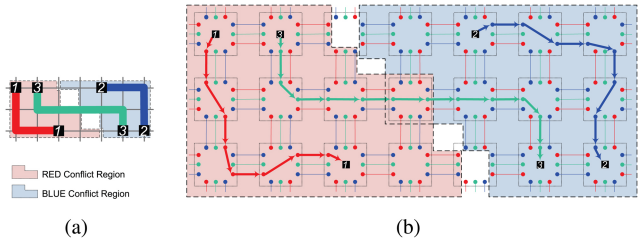


Fig. 19. Triple patterning-aware routing with expanded graph [105]. (a) Routes on the original routing grid. (b) Routes on the expanded routing graph.

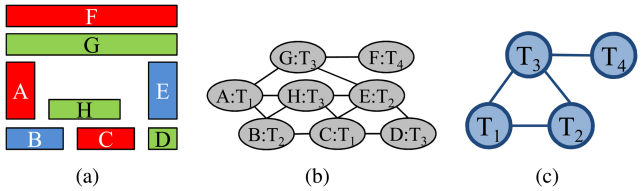


Fig. 20. TPL-aware routing with token graph to represent relative coloring relationship and the graph size. (a) TPL coloring. (b) Conflict graph and token assignment. (c) Token graph [106].

three-coloring with the objective of minimizing the total number of stitches. A special data structure, token graph-embedded conflict graph (TECG) composed of token graph (TG) and conflict graph (CG), is presented to facilitate TPL conflict detection. During path searching, [106] adopts TECG to detect if any TPL conflict occurs by the current routing wire segment. After detecting solvable TPL conflicts, TRIAD utilizes TECG to generate stitches in wire segments. With the assistance of TECG, TRIAD can generate stitches that cannot be generated by adopting conventional DPL stitch generation. TG is used to maintain the coloring relation among different vertex sets in CG. Instead of assigning physical colors into wire segments, tokens are used to represent the potential colors. In the case where three vertices comprise a three-clique, strictly colored component (SCC) is constructed to fix the coloring relation among these vertex sets in CG. Fig. 20(b) shows the TECG with one SCC $scc = (T_1, T_2, T_3)$ of the layout in Fig. 20(a). The coloring result in Fig. 20(a) can be obtained by assigning T_1, T_2, and T_3 to color c_1, c_2, and c_3, respectively, while T_4 can be assigned to c_1 or c_2. TG usually contains much less number of vertices than CG, making conflict detection more efficiently.

2) *DPL/MPL-Aware Routing for SADP:* For spacer-based multiple patterning lithography, it has, in general, a more restrictive layout requirement. It is still an open research problem how to push the limit of SADP, or even triple patterning and SAQP, to handle more general 2-D layouts with novel physical design and layout decomposition co-optimization. Note that stitch is not allowed in spacer-based MPL to resolve conflict.

An SADP-friendly detailed routing flow [107] is presented by performing detailed routing and layout decomposition concurrently. The main idea to improve the printability of routing patterns for SADP is to make pattens generated by the trim mask aligned to spacers. Therefore, [107] tried to route trim patterns around by mandrel patterns or move trim patterns away to less congested areas in the layout where addition

assist patterns can be inserted later to improve the printability. In addition, the proposed router preserves the uniformity of pattern density between mandrel and trim masks, which is simpler than the optimization for LELE-type lithography. In [108], a set of SADP-aware layout planning guidelines are presented including the following.

1) If both mandrel pattern and trim pattern are conflict-free when being assigned to a route, the mandrel pattern is preferred.
2) If the candidate routes have the same routing cost and can only be assigned as trim patterns, the route with more spacer protection is preferred.
3) The distance between a trim pattern and a mandrel pattern is suggested to be larger than the forbidden spacing, although a valid routing solution only requires the minimum spacing to be satisfied. To further resolve layout decomposition conflicts, [108] performed proper layer assignment to separate conflicting patterns. By integrating the prescribed routing patterns together with the routing cost, the router can simultaneously perform multilayer routing and layout decomposition in a correct-by-construction manner.

In [109], a new grid structure with routing rules is presented and can be applied for SADP- and SAQP-aware routing. The grid structure partially preassigns different colors to adjacent rows/columns, and the routing can be obtained by connecting two pins on grids with the same color. This approach guarantees that patterns are protected by sidewall spacers and thus has no overlay problem. However, it is less flexible since all pins and connections must lie on the grids. Most recently, [110] proposed a new SID compliant detailed router for SADP lithography. To capture the decomposition violations and SID intrinsic residue issues, a graph model is proposed and a negotiated congestion based scheme is applied to solve the overall SADP routing problem.

VI. CAD for EUV Lithography

EUVL has been delayed by multiple technology nodes. The biggest challenge for EUVL volume production is the light source, which is still one or two orders of magnitude away from the requirement of reaching 100 wafer-per-hour volume production. The light source is purely an equipment/technology issue that CAD tools cannot do much. In the following, we will discuss several unique DFM challenges for EUVL which are different from the conventional lithography. First, EUVL wavelength is 13.5 nm which is good for lithographic resolution, but flare is inversely proportional to the square of the wavelength [111]; thus, EUVL suffers a much higher flare effect caused by surface roughness and light scattering. Flare will degrade aerial image contrast and wafer pattern uniformity [112], [113]. The second major issue of EUVL is the 3-D mask effect such as mask shadowing and multilayer reflection because the EUVL system is not governed by projection masks (as in conventional optical lithography), but reflective mirroring and nontelecentric masks [114], [115]. The non-telecentric illumination of the EUV mask affects feature imaging, which needs to be carefully considered in EUV lithography modeling [116], [117]. Other key issues with EUVL include line edge roughness (LER) [118], [119] and mask defects. It is necessary to extract and model the first-order effects of these variations/defects and use them to guide EUVL proximity correction and EUVL-aware physical design.

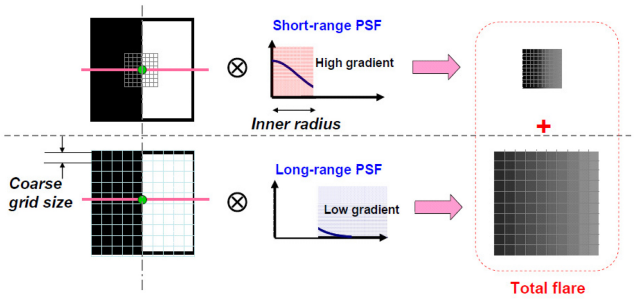


Fig. 21. Total (short and long range) flare kernels in EUV lithography [111].

A. EUV Flare Modeling and Mitigation

It is important to model the variations and defects of EUVL accurately so that the model can be used to guide EUVL proximity correction and EUVL-aware physical design. Several challenging factors for full-chip EUVL modeling, flare, LER, and 3-D mask effects are discussed as follows.

Flare effect strongly depends on the pattern density. The flare effects can be long-range, medium-range, and short-range flare [120]. To compute the overall flare effect, a point spread function (PSF) derived from the surface roughness of the EUV optics can be applied, which can be fitted with a Gaussian function [121], [122]. Then, the aerial image $I(x, y)$ on wafer can be calculated as follows:

$$\begin{aligned} I(x, y) &= I_0(x, y)(1 - C) + I_{flare}(x, y) \\ I_{flare}(x, y) &= I_0(x, y) \otimes PSF \end{aligned} \tag{9}$$

where $I_0(x, y)$ is the areal image without flare, $I_{flare}(x, y)$ is a local flare intensity, and C is a normalization factor to compensate for energy conservation.

A multigrid structure to model the multirange flare effects is shown in Fig. 21. Flare contributions from short distances in PSF can be modeled with fine grids because the short range PSF has high gradients, while long range contributions can be calculated with coarser grids. The total flare contribution can be obtained by summing up the multirange effects [111].

One flare compensation strategy is to perform dummification [121], [123] to mitigate the flare effect, where dummy patterns are added to the layout area according to the flare distribution. Recently, [124] proposed a simultaneous flare level and flare variation optimization with dummification. Given a grid-based mask layout, a fast error-controlled flare map is first computed, and then the dummification process is performed using a quasi-inverse lithography technique. The dummification process consists of two stages: 1) global dummification, where dummy is assigned top-down to simultaneously optimize flare level and flare vibration, and 2) local refinement, where flare variation is further minimized in a greedy manner.

More research will be required to model EUVL effects accurately in full-chip scale, such as multirange flare modeling;

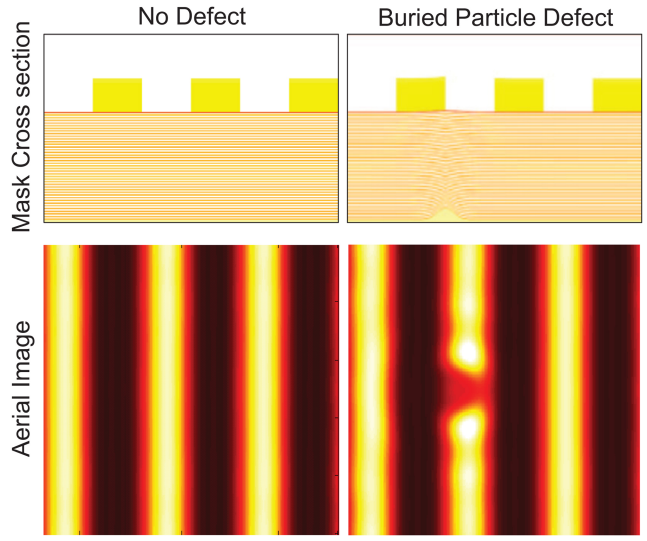


Fig. 22. EUV buried defect on a mask and the simulated aerial images [126].

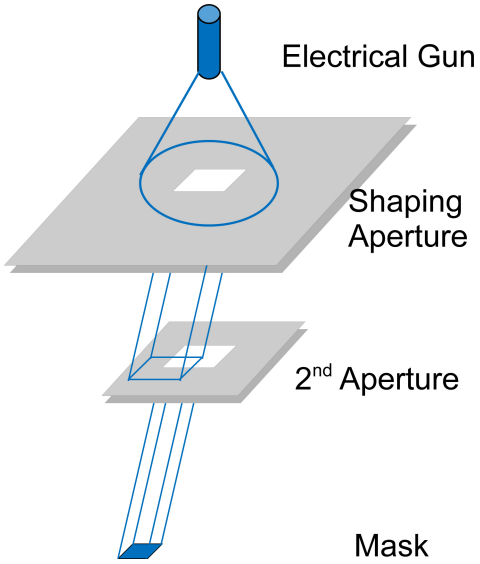


Fig. 23. Variable shaped beam (VSB) is a conventional EBL technique.

3-D mask effect modeling considers layout-dependent variations, and so on. These models can then be used for EUVL-aware proximity corrections and layout optimizations.

B. EUV Blank Defect Mitigation

Currently, making a defect-free EUV mask blank is still too costly and impractical, which is one of the main challenges for EUVL mask fabrication. The main problem is the buried defect on the blank with multilayer reflecting structures. A EUV mask example is shown in Fig. 22. Buried defects may be caused by: 1) pits on the substrate surface, or 2) particles that are introduced on the substrate surface or during multilayer deposition. Although a mask marker can be used to reduce the density of buried defects, the accuracy of most inspection tools is still questionable. According to [125], there are many problems with the detection of defect locations where 10–30 nm inaccuracy is observed, and the inspection throughput is still far from the requirement. On the other hand, buried defects can be partially repaired by e-beam. However, there is a risk of damaging the multilayer structure. Therefore, it is necessary to develop a method to defective EUV mask blanks.

One approach to solve EUV blank defects is to move the mask patterns such that defects can be avoided. Burns *et al.* [127] first presented the pattern shifting and rotation process to mitigate defects using a simple enumerative technique. Zhang *et al.* [128] proposed an efficient layout relocation process to minimize the defect impact on feature boundaries. The idea is to shift the pattern on the blank and move the defects to the spare region where the printing image will not be affected. The pattern relocation problem is formulated into a rectangle overlapping problem and can be optimally solved. The experimental results showed that the patterns affected by the defects can be very much reduced. The follow-up study [129] further improves the performance to find all relocation positions throughout the entire blank. The algorithm first partitions the exposure field into rectilinear regions based on the defect positions and the die size. Then, the algorithm finds all relocation positions for each region in linear time.

In reality, there will be multiple copies of a die on a blank, and each die is allowed to be relocated individually to mitigate defect impact. The reticle floorplanning technique [130] is proposed based on a simulated annealing approach to minimize the design impact of buried defects for single-project reticles. A defect-aware multidie placement algorithm for EUV mask is developed in [131]. For a given die size and a defective blank, the algorithm maximizes the number of dies that can be placed within the exposure field such that the defect impact is completely avoided. The experimental results revealed an important tradeoff between the placement freedom and the mask failure tolerance, which deserves a special attention.

VII. CAD for E-Beam Lithography

EBL [132], [133] is one of the most promising candidates for the next-generation lithography technologies, along with EUVL. Compared with the traditional lithographic methodologies, EBL has several advantages.

1) Electron beam can be easily focused onto nanometer diameter with charged particle beam, which can avoid suffering from the diffraction limitation of light.
2) The price of a photomask set is getting unaffordable. As a maskless technology, EBL can reduce the manufacturing cost.
3) EBL allows a great flexibility for fast turnaround times and even late design modifications to correct or adapt a given chip layout.

Because of all these advantages, EBL is widely deployed in mask making, small volume LSI production, and research and development to develop the technological nodes ahead of mass production.

Variable shaped beam (VSB) is a conventional EBL technique, and its printing process is illustrated in Fig. 23. First, an electrical gun generates initial beam, which becomes uniform through the shaping aperture; then, the second aperture finalizes the target shape with a limited maximum size. In the

VSB mode the whole layout should be decomposed into a set of nonoverlapping rectangles, through a process called layout fracturing. At the 22-nm logic node and beyond, because of the design shrink and the inverse lithography techniques or OPC, the total e-beam shot for each mask count could be larger than 1T [134]. Therefore, the low throughput has been and still is the main limitation of the EBL technique.

To overcome the throughput issue, several optimization methods have been proposed to reduce the EBL writing time to a reasonable level. In the following, we will survey some solutions to improve the writing time of EBL system.

A. Layout Fracturing for Throughput Improvement

As discussed above, one of the most critical steps in EBL writing process is the layout fracturing, where the layout pattern is decomposed into numerous nonoverlapping rectangles or triangulars. Subsequently, all the rectangles are prepared and exposed by EBL writing machines, where each fractured rectangle is shot by one electron beam. Note that small size feature, denoted as sliver, may lead to an increase in the mask error enhancement factor (MEEF) [135]. Since an increase of MEEF will cause larger CD variation or more manufacturing defects, either the number of slivers or the total length of slivers should be minimized. Because of the sliver issue, the layout fracturing problem is distinct with the polygon decomposition, in general, geometrical science. There are several works for the layout decomposition problem [136]–[138].

It will be noted that as the minimum feature size further decreases the number of shapes to be printed will be steadily increased, which may cause the low throughput problem. To overcome this problem, different strategies have been proposed to reduce the EBL writing time. One method is called model based fracturing, where the input layout is decomposed into circles and overlapping is accommodated [139], [140]. Another technique is called L-shape shot strategy, where L-shape beams can be written in one shot [141]–[143]. It will be noted that although one more aperture is needed, the L-shape shot strategy has the potentiality to reduce the EBL writing time or cost by 50% if all rectangles are combined into L-shapes.

B. Design for Character Projection

To improve the throughput, recently another new technique, called character projection (CP), has been proposed. The main idea of CP is that some complex shapes or characters can be prepared on a stencil and each character can be printed in one shot. For those shapes that cannot find matching characters on the stencil, they have to be decomposed into VSBs. During manufacturing, any layout pattern that can be found on the stencil will be chosen and directly projected into the mask/wafer in one shot. Due to less beam shots for the same layout, the CP system has much higher throughput than VSB. However, only a limited number of character candidates can be employed, because of the area constraint of the stencil. For modern design, it is not practical to fully make use of CP due to numerous distinct circuit patterns. Those patterns, not contained by any character, are still required to be written by VSB [144].

Although the CP mode can effectively reduce the EBL writing time, it introduces a more design challenge to the CAD flow. It is intuitive that commonly used circuit patterns should be selected as characters for minimizing the total number of shots, hence projection time and throughput. Sugihara *et al.* [145] provided an algorithm for the technology mapping problem to generate the repeating patterns. These repeating patterns are extracted from the mask data after OPC [146]. Besides, during standard cell design and routing stages, some constraints are introduced to generate CP friendly patterns [147], [148].

In addition, one design step, called stencil planning, is provided to take advantage of the CP mode. First, this step solves the scheduling of character candidates between the VSB mode and the CP mode. Besides, the relative locations of characters are considered. The character sizing problem is handled in [149]. In [150] and [151], the stencil planning was viewed as a character selection problem, where ILP is applied to select a group of characters for minimizing total projection time. For each character, blanking spaces are usually reserved around its enclosed rectangular circuit pattern. Yuan *et al.* [152] considered the overlapping of characters in the stencil planning. Du *et al.* [153] proposed a series of methods, including character design, stencil compaction, and layout matching for CP based EBL. An area-efficient stencil design was presented for the CP improvement of VIA patterns, where each character can contain at most three VIAs. Recently, Ikeno *et al.* [154] adopted 1-D VIA arrays architecture to increase VIA numbers for each character, while saving the stencil area by superposed characters. Besides, CP throughput is further improved by layout constraints for VIA arrangement. To further overcome EBL throughput limitation, a multicolumn cell (MCC) system was proposed as an extension to the conventional CP, where several independent CPs are used to further speed up the writing process. In [155], a set of algorithms were proposed to solve the overlapping-aware stencil planning problems for the MCC system.

C. Other Design Challenges

Apart from the throughput issue, several other design problems are involved in EBL design flow. Here, we list two of them: subfield scheduling and massively parallel writing.

In EBL design flow, most of the beam energy is released as heat and accumulates in the local area of writing. Resist heating has been identified as a main contributor to CD distortion in EBL writing [156]. To solve the heat problem, one solution is called subfield scheduling, which reorders the sequence of the layout writing process to avoid the successive writing of subfields that are close to each other. Babin *et al.* [156] proposed a Lagarias based scheduling, and [157] presented a greedy-based improvement. Recently, Fang *et al.* [158] formulated the problem into a constrained maximum scatter traveling salesman problem (constrained MSTSP). Although the general constrained MSTSP problem is NP-hard, they identified a special case that can be solved optimally in linear time. A framework was proposed which first decomposed

the problem into a set of subproblems, and then merged all subsolutions together.

Massively parallel EBL writing is under active research and development for high throughput e-beam lithography. Recently, several industry EBL writing tools, i.e., MAPPER [159] and REBL [160], have applied the parallel writing technique. However, it is not clear what CAD issue will be important for the massively parallel e-beam writing until the equipment/technology reaches some maturity.

VIII. Conclusion

In this paper, we have surveyed key design for manufacturability issues with emerging nanolithography technologies, including DPL/MPL, EUVL, and EBL. We first illustrate the fundamental of lithography modeling and analysis, which can be used for post-lithography geometrical image simulations, electrical analysis, as well as optical proximity correction. Note that detailed lithography simulations are very computationally expensive, and are thus difficult to be used in inner loops of early physical design stages. To raise the level of abstraction, modern lithography hotspot detection techniques that provide a faster hotspot identification based on pattern matching and machine learning are discussed. We then demonstrate the challenges of mask synthesis and discuss how modern RET techniques can improve the printability. To scale further with the 193-nm lithography, double/multiple patterning lithography has been widely used. There are two mainstream processes, LELE and SADP, which will put different constraints and requirements to the layout. Layout decomposition is a fundamental problem for DPL/MPL, and we have discussed various studies to minimize conflict and stitch, balance the mask density, and control the overlay.

With further scaling of feature size into very deep subwavelength, the mask-level manipulation conventionally performed at the fab is limited if the physical design sent to the fab is not lithography friendly. It is necessary to integrate lithography awareness into nanometer VLSI physical design flow to ensure high manufacturability. Several lithography-friendly physical design challenges and recent studies including routing, standard cell design, and placement are presented. Tight physical design and technology co-optimization is mandatory to make the further scaling worthwhile. This may call for new cell and routing design architectures that favor very regular fabrics and reconfigurability.

While the immediate technology nodes such as 22 nm and 14 nm will still be mainly using 193-nm immersion lithography, alternative lithography technologies such as EUVL, EBL are under heavy research and development. They all have their own technology challenges and CAD opportunities, e.g., flare effects and mask defect for EUV, throughput for EBL, and ultraregular layout for DSA [161]. In the longer horizon, hybrid lithography [76] will be very interesting for ultimate nanopatterning, e.g., DPL/MPL with e-beam cutting [77]–[79], DSA with EBL, EUV with MPL, and so on. The DFM research for hybrid lithography is still wide open for ultimate patterning with acceptable cost. No exponential scaling can be forever. As the feature size scaling slows down or stops at the end, other equivalent scaling, such as 3-D IC integration, new material and devices, and new architecture and design paradigms, will still have a lot of room to improve and continue the equivalent Moore's law benefit.

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