Design for Manufacturability: From Ad Hoc Solution To Extreme Regular Design

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1 Introduction and Motivation

In very large scale integrated (VLSI) circuit design, shrinking transistor feature size using advanced lithography techniques has been a holy grail for the whole semiconductor industry. However, the gap between the manufacturing capability and the design expectation becomes more and more critical for sub-28nm technology nodes Under the constraint of 193nm wavelength lithography, advanced circuit designs are vulnerable to many reliability issues, such as open/shorts, performance degradation, or parametric yield loss. There are several lithography techniques to overcome these issues [1]. In emerging technology node and the near future, multiple patterning lithography (MPL) has become the most viable lithography technique. Generally speaking, MPL consists of two different manufacturing processes: litho-etch type and self-aligned patterning type. In the longer future (for the logic node beyond 14nm), there are several next generation lithography options, such as extreme ultra violet (EUV), electron beam lithography (EBL), directed self-assembly (DSA), and nanoimprint lithography (NIL).

Design for manufacturability (DFM), in conjunction with process integration challenges, are being actively research, to provide friendliness to these lithography techniques. For MPL, there are intensive investigations to solve layout decomposition, where the input layout is divided into several masks (e.g. [2–6]). Besides, some research work considers particular MPL constraints in early design stage, such as placement [7, 8] and routing [9–11]. For EUV, to migrate the mask blank defect, layout patterns are relocated to avoid the defect impact [12]. Also, related design constraints to avoid blank defect can be integrated into early physical design stage (e.g. [13]). For EBL, since its key limitation is the low throughput, many approaches have been developed to improve the system throughput [14–16]. For DSA, how to design and verify the guiding template patterns, which form DSA holes insides, have been investigated in [17] and [18], respectively.

However, so far most of the DFM research are merely providing ad hoc solutions. That is, one specific work is targeting at one particular lithography constraint, and one work is hard to be re-used by another one where a new lithography constraint is involved. Therefore, CAD vendors may have to prepare a bunch of technical supports to these emerging design challenges. Recently there is a trend that different lithography techniques may combined to provide better printability (e.g., MPL+EBL [19] and MPL+DSA [20]). Due to such trend, in the near future, the situation may be even worse that more and more CAD tools and design supports are required.

Extreme regular design is a promising solution for DFM community to resolve the diverse design challenges [21, 22]. Fig. 1 gives an example of such extreme regular layout [23], where we can see that the layout can be decomposed into line patterns and cut patterns. The benefit of such regularity is twofold. On the one hand, although various resolution enhancement techniques (RET) are utilized, random geometrical configurations are still hard to implement due to lithography limitation. Extreme regular style is able to

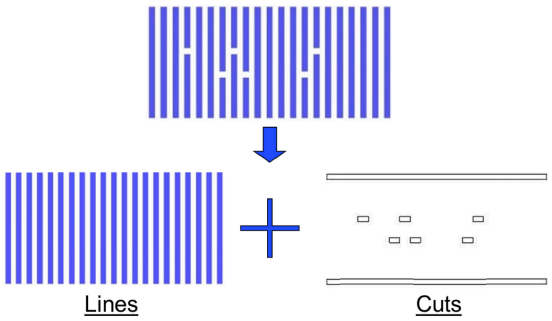

Figure 1: Regular design can be decomposed into lines and cuts [23].

improve the manufacturability and achieve manageable post-layout processing complexity. As shown in Fig. 1, the regular layout is the ease of splitting into line patterns and cut patterns. This allows independent process optimization of the line patterns and cut patterns. On the other hand, extreme regular design is naturally friendly to different emerging lithography techniques. For example, the cut patterns can be easily manufactured using EBL, DSA, or MPL.

2 Current Research for Extreme Regularity

2.1 Standard Cell Design Stage

Standard cell design is a critical stage for providing overall layout regularity. There have been some cell synthesis works for regular standard cells [24–27]. However, while the yield and performance benefits of regularized layouts may be well accepted, the biggest barrier to broader implementation of regularized layout styles is the perceived impact on layout density and intra-cell routability [28]. Recently, a Tungsten-based middle of line (MOL) structure is introduced to connect intra-cell transistors [29]. MOL structure is made up of two different local interconnection layers, CA and CB (sometimes called IM1 and IM2, respectively), where the CA layer is used as a connection layer for active fins and better landing for the contacts in active region, while the CB layer is mostly used for via landing and gate shortening [30].

Ye et al. [31] studied the problem of cell layout regularity optimization under MOL structure. Fig. 2 gives an example of the proposed cell optimization, where the input 2D cell in older technology node is shown in Fig. 2(a), while the optimized unidirectional cell is in Fig. 2(b). Due to the unidirectional shapes of MOL and Metal-1 layers, the patterns are SADP friendly. That is, the line-space array decomposition can be applied to SADP with trim masks, with tight control on overlay and wafer-print artifacts. A general integer linear programming (ILP) formulation is proposed to solve the unidirectional cell optimization under MOL structure. Besides, a set of hybrid techniques is presented to search for high quality cell optimization solution.

Several works have been done on the investigation of contact layer fabrication and contact layer optimization. Yi et al. [32] demonstrated the fabrication of DSA contacts for regular standard cells. Besides, Du et al. [17] proposed a DSA aware contact layer optimization method for regular standard cell design. By assigning cost function to different DSA templates based on their manufacturability, they optimized the DSA aware contact layer. Recently, Ou et al. [33] performed a comprehensive investigation on the DSA based end-cutting problem, where a mathematical formulation is proposed to search for minimum wire extensions and minimum conflicts for all test cases.

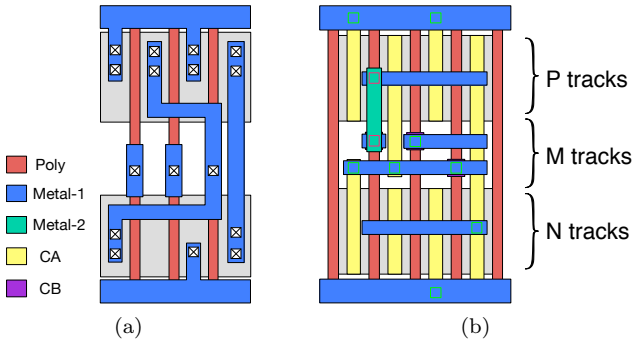

Figure 2: Example of cell regularity optimization in [31]. (a) The input layout with ten tracks. (b) The optimized layout with nine tracks.

2.2 Detailed Routing Stage

Detailed routing aims at pin access and search for exact routes of each net. A typical detailed routing strategy performs pathfinding of the nets sequentially. [34, 35] proposed a comprehensive framework to explicitly address the regular routing under regular layout constraints. Fig. 3 illustrates an example of such regular detailed routing result. The wafer image quality of irregular 2D line-end cut patterns in Fig. 3(c) suffers from more severe pattern distortion than that of 1D cut patterns in Fig. 3(e) [35].

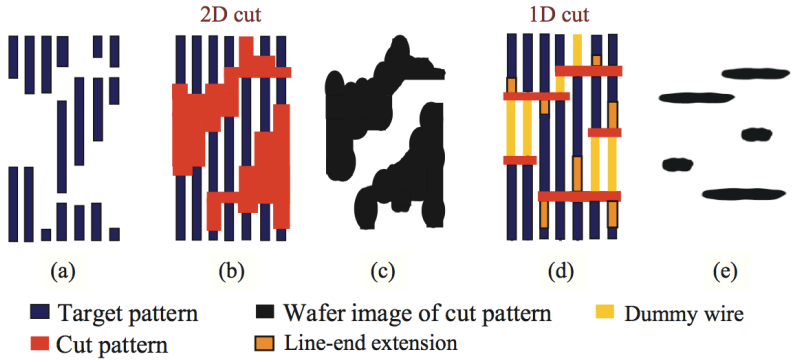

Figure 3: The 1D target patterns in (a) can be formed by a 1D nanoarray with (b) 2D irregular or (d) 1D regular line-end cut patterns. (c) The wafer images of 2D irregular cut patterns suffer from distortion and degrade the printability of line ends. (e) The wafer images of 1D regular cut patterns have better line-end printability [35].

3 Future Work

There are a large amount of emerging design challenges, along with the regular design style. Here I list three of them.

- Firstly, due to limited local routing resources and dense I/O pins, pin access is still a serious problem for detailed routing. To overcome the local congestion problem, physical design tools should be aware of the congestion derived from the dense I/O pin cells. For instance, in placement stage local congestion

mitigation can be applied to prevent placing hard-to-routed cells too close together [36]. More importantly, the standard cell library should be carefully designed to enhance the pin accessibility. That is, I/O pins need to be balanced distributed within a cell, as the alignment or the densely packing of pins make the cell more difficult to be accessed.

- Secondly, under regular design style, alghough the printability and yield is improved, one standard cell may suffer from area and timing penalty. How to optimize the cell layout while timing constraints are satisfied is a critical problem.

- Thirdly, a coherent physical design framework is imperative. Although there are some attempts on extreme regular routing (e.g. [34, 35]), how to handle the extreme regular design style across the placement and routing stage is still an open problem.

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