Routability-Driven and Fence-Aware Legalization for Mixed-Cell-Height Circuits

Haocheng Li[1], Wing Kai Chow[2], Gengjie Chen[1], Evangeline F. Y. Young[1], Bei Yu[1]

[1]The Chinese University of Hong Kong

[2]Cadence Design System Inc.

香港中文大學
The Chinese University of Hong Kong

cadence®

Outline

Outline

Motivation

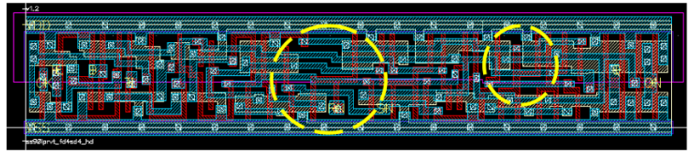


Figure 1: Large Single-Row Cell [Baek et al. 2008]

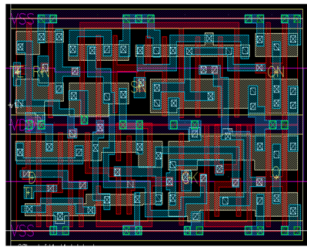


Figure 2: Multi-Row Cell [Baek et al. 2008]

- Cells like multi-bit flip-flops (MBFFs) occupy multiple rows [a].
- Cells are much more accessible by being modified to be multi-row height [b].

[a] [Lin, Hsu, and Chang 2011]
[b] [Raghavan et al. 2016]

Legalization

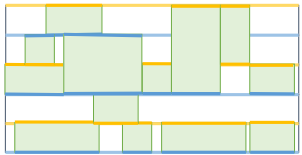


Figure 3: Power/ground alignment.

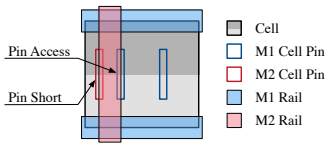


Figure 4: Pin access and pin short.

Objective function [a]:

$$S_{am} = \frac{1}{H}\sum_{h=1}^{H}\frac{1}{|C_h|}\sum_{c_i \in C_h}\delta_i, \tag{1}$$

where $\delta_i = \delta_{x_i} + \delta_{y_i} = |x_i - x_i'| + |y_i - y_i'|$, satisfying [b]:

- Cells are overlap-free;
- Cells are aligned to placement sites.
- Cells with height of even multiples of site height must be placed in alternate rows with matching power and ground alignment.
- Signal pins of cells should not be short or inaccessible due to the P/G grids and IO pins [c].

[a] [Darav, Bustany, et al. 2017]
[b] [Chow, Pui, and Young 2016]
[c] [Darav, Kennings, et al. 2016]

Detailed Placement Flow

The detailed placement consists of three stages.

- Inserts the cells sequentially into the placement region.
- Optimize the maximum displacement by swapping cells.
- Further optimize the average and maximum displacement.

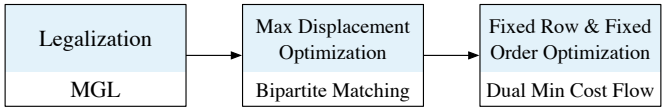


Figure 5: Detailed placement flow.

Outline

[Chow, Pui, and Young 2016]

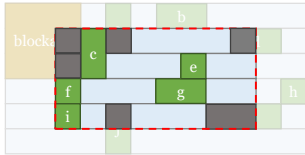


Figure 6: Local Region

- Define local region
- Enumerate insertion points
- Evaluate cost
- Spread overlapping cells

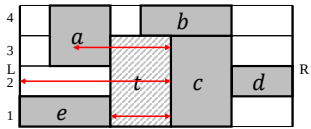


Figure 7: Insertion Point

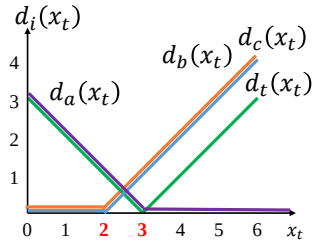
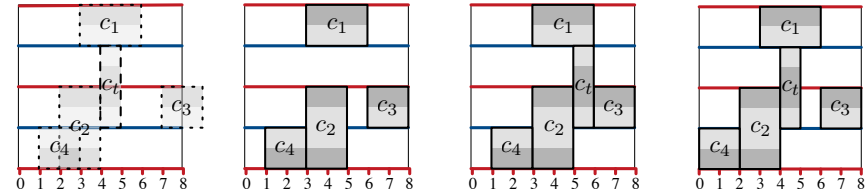


Figure 8: Cost Evaluation

Difference between MLL & MGL



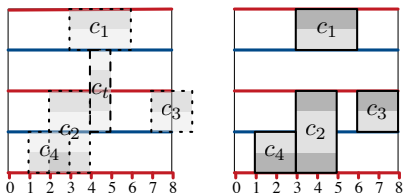
(a) Global Placement (b) Local Region (c) MLL (d) MGL

Figure 9: Comparison between MLL and MGL.

MLL optimizes the total displacement from the initial positions of the cells in the window before calling MLL.

MGL minimizes the displacement from the respective positions of cells obtained after global placement.

Clustered Cells



(a) Global Placement (b) Local Region

Figure 10: c_2 and c_4 form a cluster.

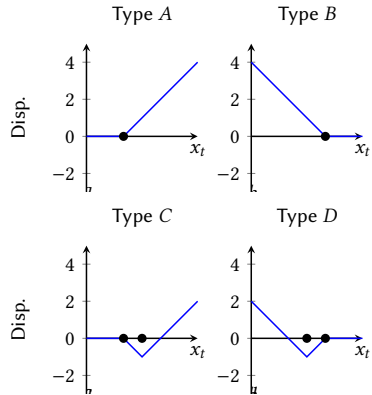
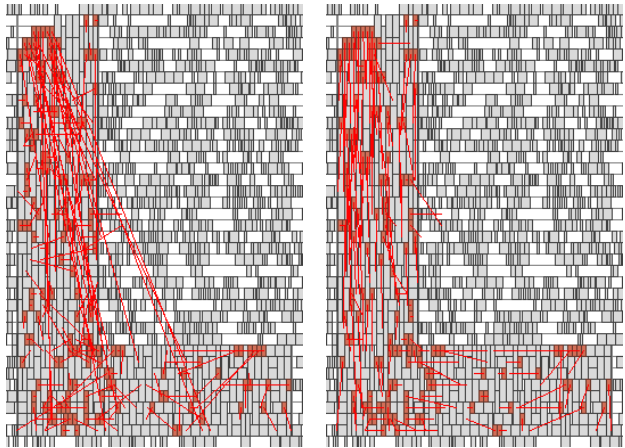


Figure 11: Cost Curve Types A – D.

Outline

Bipartite Matching



(a) Before (b) After

Figure 12: Bipartite matching.

Outline

[Vygen 1998]

- Fixed-row and fixed-order.
- Minimizes the half-perimeter wire length (HPWL).
- A dual of min-cost flow problem.

Fixed Row & Fixed Order Optimization

Formulate linear displacement:

$$\max_{x_i, x_i^-, x_i^+} \sum_i n_i(x_i^- - x_i^+) \tag{2}$$

$$\text{s.t. } x_i^- \le x_i - x_i' \le x_i^+, \qquad \forall c_i \in C, \tag{2a}$$

$$x_i^- \le 0 \le x_i^+, \qquad \forall c_i \in C, \tag{2b}$$

$$x_i - x_j \le -w_i, \qquad \forall (i,j) \in E, \tag{2c}$$

$$l_i \le x_i \le r_i, \qquad \forall c_i \in C. \tag{2d}$$

Let $\tilde{x}^0$ be the absolute position of the *origin*, then the absolute positions $\{\tilde{x}_i, \tilde{x}_i^-, \tilde{x}_i^+\}$ of $\{x_i, x_i^-, x_i^+\}$ are $\tilde{x}_i = x_i + \tilde{x}^0$, $\tilde{x}_i^- = x_i^- + \tilde{x}^0$, $\tilde{x}_i^+ = x_i^+ + \tilde{x}^0$. Thus,

$$\max_{\tilde{x}_i, \tilde{x}_i^-, \tilde{x}_i^+, \tilde{x}^0} \sum_i n_i(\tilde{x}_i^- - \tilde{x}_i^+) \tag{3}$$

$$\text{s.t. } \tilde{x}_i^- \le \tilde{x}_i - x_i' \le \tilde{x}_i^+, \qquad \forall c_i \in C, \tag{3a}$$

$$\tilde{x}_i^- - \tilde{x}^0 \le 0 \le \tilde{x}_i^+ - \tilde{x}^0, \qquad \forall c_i \in C, \tag{3b}$$

$$\tilde{x}_i - \tilde{x}_j \le -w_i, \qquad \forall (i,j) \in E, \tag{3c}$$

$$l_i \le \tilde{x}_i - \tilde{x}^0 \le r_i, \qquad \forall c_i \in C, \tag{3d}$$

whose dual linear programming is a min-cost flow problem.

Example of Min-Cost Flow

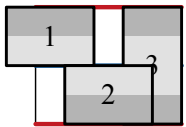


Figure 13: GP.

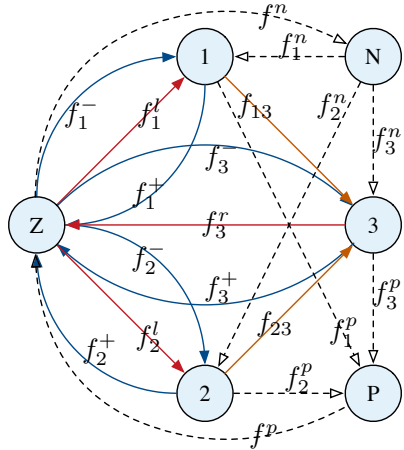
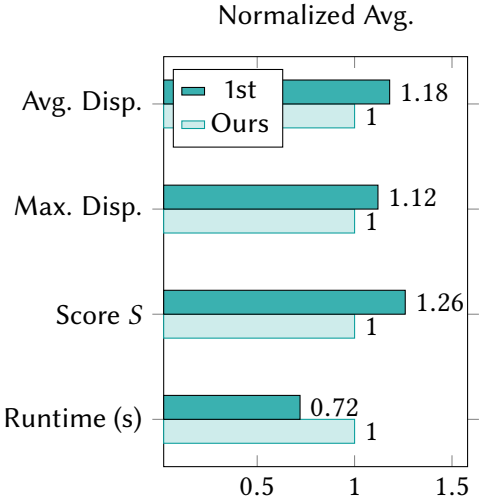
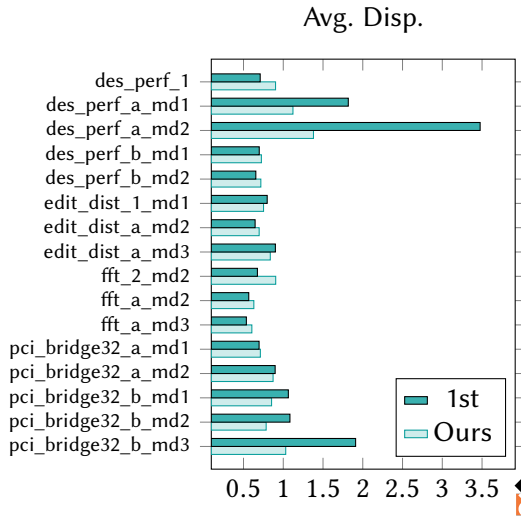


Figure 14: Flow network.

Outline

Experimental Results





Outline

Conclusion

- Propose multi-row global legalization.
- Adjust the maximum displacement by bipartite matching.
- Formulate the fix-row-and-order legalization into a minimum-cost flow problem.
- Comparing with the champion of the ICCAD 2017 Contest, we achieved 18% less average displacement, 12% less maximum displacement, and much fewer routability-driven violations.

Thanks!

Questions?

References I

- Baek, Sang-Hoon, Ha-Young Kim, Young-Keun Lee, Duck-Yang Jin, Se-Chang Park, and Jun-Dong Cho (2008). "Ultra-high density standard cell library using multi-height cell structure". In: *Proceedings of SPIE*. Vol. 7268.
- Chow, Wing Kai, Chak Wa Pui, and Evangeline F. Y. Young (2016). "Legalization Algorithm for Multiple-Row Height Standard Cell Design". In: *ACM/IEEE Design Automation Conference (DAC)*, 83:1–83:6.
- Darav, Nima Karimpour, Ismail S. Bustany, Andrew Kennings, and Ravi Mamidi (2017). "ICCAD-2017 CAD Contest in Multi-Deck Standard Cell Legalization and Benchmarks". In: *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, pp. 867–871.
- Darav, Nima Karimpour, Andrew Kennings, Aysa Fakheri Tabrizi, David Westwick, and Laleh Behjat (2016). "Eh? Placer: a high-performance modern technology-driven placer". In: *ACM Transactions on Design Automation of Electronic Systems (TODAES)* 21.3, p. 37.

References II

- Lin, Mark Po-Hung, Chih-Cheng Hsu, and Yao-Tsung Chang (2011). “Recent research in clock power saving with multi-bit flip-flops”. In: *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. 1–4.
- Raghavan, Praveen, F Firouzi, L Matti, P Debacker, R Baert, SMY Sherazi, D Trivkovic, V Gerousis, M Dusa, J Ryckaert, et al. (2016). “Metal stack optimization for low-power and high-density for N7-N5”. In: *Design-Process-Technology Co-optimization for Manufacturability X*. Vol. 9781. International Society for Optics and Photonics, 97810Q.
- Vygen, Jens (1998). “Algorithms for detailed placement of standard cells”. In: *IEEE/ACM Proceedings Design, Automation and Test in Europe (DATE)*, pp. 321–324.