Test Wrapper Design and Optimization Under Power Constraints for Embedded Cores With Multiple Clock Domains

Qiang Xu, Nicola Nicolici, and Krishnendu Chakrabarty

***Abstract*—Even though many embedded cores contain several clock domains, most published methods for wrapper design have been limited to single-frequency cores. Cumbersome and invasive design techniques, such as insertion of test points, are needed to make these methods applicable to current-generation embedded cores. This paper presents a new method for designing test wrappers for embedded cores with multiple clock domains. The proposed 1500-compliant wrapper prevents clock skew and allows scan chains in different clock domains to shift test data at distinct clock frequencies, which enables a better control of power dissipation during test. We present an integer linear programming (ILP) model that can be used to minimize the core testing time under power constraints for small problem instances, and which can be combined with LP-relaxation to obtain lower bounds on the testing time for larger instances. We also present an efficient heuristic method that is applicable to large problem instances, and which yields the same (optimal) testing time as ILP for small problem instances.**

***Index Terms*—Embedded core, multifrequency, test wrapper.**

I. Introduction

Modern system-on-a-chip (SOC) uses embedded cores that operate internally with multiple clock domains (e.g., [1]). In addition, some cores may operate internally at very high rates, typically employing phase-locked loops (PLL) to generate on-chip clocks from far slower external reference signals. For these high-performance cores with increasing number of clock domains, there are two major test challenges: 1) traditional techniques (e.g., I_{DDQ} and functional testing) used for detecting timing-related defects are less effective [2] and 2) clock skew during test might corrupt test data and render the test useless [3]. Therefore, to ensure a high quality of defect screening, it is essential that core tests can be conducted at rated-speed without clock skew problems. At the same time, since a circuit may consume more average power and/or peak power in test mode than in normal mode, low-power dissipation during test application is becoming increasingly important [4], [5].

To the best of our knowledge, [6] provides the only strategy in the literature for at-speed testing of cores with multiple clock domains using an IEEE Std. 1500-compliant wrapper [7]. A limitation of this paper, however, lies in the fact that different clock domains share the same clock signal during the scan shift phase. On the one hand, if this shift frequency is too low, the core test application time (TAT) might become prohibitively high. On the other hand, if this shift frequency is too high, the elevated average test power might cause structural damage to the circuit under test (CUT). Clearly, the selection of the single shift frequency directly impacts the tradeoff between the average power consumption and scan time, and excessive TAT may result under given average power constraints. In addition, if all the flip-flops update their states on the same clock edge during scan shift phase, the simultaneous switching noise can cause a large voltage drop that may lead to erroneous data transfer, thus invalidating the testing process [5].

To tackle the above problems, in this paper, we propose a power-constrained wrapper design for cores with multiple clock domains. When compared to [6], the main contributions of this paper are as follows.

1) The proposed wrapper design enables each clock domain to operate at a distinct shift frequency during test, which opens more room for the wrapper optimization process. In addition, the embedded core test is controlled solely on-chip without requiring external scan enable signal provided from the automatic test equipment (ATE). The saved test control pins can then be utilized to transfer test data to further reduce testing time.
2) In order to optimize the proposed wrapper in terms of testing time under power constraints, we present an integer linear programming (ILP) model that can be used for small problem instances, and which can be combined with LP-relaxation to obtain lower bounds on the testing time for larger instances. We also present an efficient and effective heuristic method that is applicable to large problem instances with near-optimal solutions.

One of the limitations of the proposed method is that it is tailored for embedded cores with fixed scan chains, and hence it is less effective for designs where the core internal scan chains are flexible during system integration. In addition, we assume each scan chain contains flip-flops from only one clock domain. If this is not the case, only one of the clock domains on a scan chain can be tested at its rated speed.

The rest of this paper is organized as follows. In Section II, the related work in this domain is surveyed. Section III describes the new scan control unit design which supports multiple shift frequencies for different clock domains. In Section IV, two wrapper optimization techniques are presented. Next, Section V shows our experimental results for two multifrequency cores. Finally, Section VI concludes this paper.

II. Related Work

A. Multifrequency At-Speed Testing

Many solutions for scan-based at-speed testing have been introduced and are gaining industry acceptance recently [2], [8]. The basic idea is to generate at-speed test clock pulses on-chip for the launch and capture events, while the other shift cycles are pulsed at lower speed to control the test power. In addition, several techniques have been proposed to test designs with multiple clock domains. In [9] and [10], Nadeau-Dostie *et al.* proposed two different techniques to avoid clock skew during test. However, since scan chains are shifted at their corresponding functional frequencies in both solutions, they are impractical for today's high-speed design. Schmid and Knablein [11] introduced extra latch/flip-flop in between transition-hazard clock domains to avoid the clock skew problem. The two-phase clocking scheme that they used, however, can only be applied for low-frequency scan test. Bhawmik [12] and Hetherington *et al.* [13] employed rather different approaches that separate the clocking for shift and capture in two phases, by multiplexing the clock signals for each phase. Careful

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Q. Xu is with the Department of Computer Science and Engineering, Chinese University of Hong Kong, Shatin, N.T., Hong Kong (e-mail: qxu@cse.cuhk.edu.hk).

N. Nicolici is with the Department of Electrical and Computer Engineering, McMaster University, Hamilton, ON L8S 4K1, Canada.

K. Chakrabarty is with the Department of Electrical and Computer Engineering, Duke University, Durham, NC 27708 USA.

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capture windows are designed to avoid clock skew problems, while the shift operation can work at any of the on-chip frequencies.

B. Low-Power Testing

A circuit generally consumes more power (including both average power and peak power) in the test mode than in the normal mode of operation [5]. To cope with this problem, extensive research has been done to reduce test power [4], [5].

For core-based SOC testing, usually system integrators are given test cubes for each intellectual property (IP) core without its structural information. To reduce core test power in this situation, Sankaralingam *et al.* [14] proposed a low-power static test compaction technique by carefully selecting the merging order of the test cube pairs. Chandra and Chakrabarty [15] used Golomb codes to encode core test vectors, which reduces both test data volume and scan power dissipation. Different from the above, this paper considers the *ad hoc* technique that reduces test power by simply decreasing scan shift frequency. This is not a new concept, nonetheless, the key to our method is that we try to assign shift frequency for each clock domain intelligently so that the testing time can be minimized under a given power constraint. This is not incompatible to the other low-power testing techniques that manipulate test cubes, and hence can be effectively combined with them to further reduce test power. In addition, although this multifrequency testing strategy is mainly used to control the average power consumption during the scan shift phase, it can be also used to reduce the instantaneous scan shift power, by introducing a phase difference between the shift clocks used for different clock domains.

C. Wrapper Design and Optimization

Core test wrapper is a thin shell around a core that facilitates the core and its environment to be tested independently. Its interface has been standardized by the IEEE Std. 1500 [7], but the internal structure can be designed differently based on a specific SOC test requirement. The design and optimization of core test wrapper mainly involves the construction of balanced wrapper scan chains (WSCs), which usually comprises a number of wrapper boundary cells and/or core internal scan chains. Many test wrapper architectures and the associated wrapper optimization algorithms have been proposed in the literature (e.g., [16] and [17]). However, they are only applicable to single-frequency embedded core test. Cumbersome and invasive design techniques such as the insertion of test points (e.g., antiskew latches and fault masking circuits) are needed to make these techniques applicable to current-generation embedded cores. The IEEE Std. 1500 also does not provide any direct or noninvasive support for the modular testing of cores with multiple clock domains. The multifrequency wrapper proposed in [6] effectively solved the clock skew problem for at-speed testing embedded cores with multiple clock domains. In this paper, logic blocks belonging to different clock domains are grouped as different virtual cores (VCs). For each VC, a single-frequency virtual wrapper,[1] containing the WSCs for the respective group, is assigned. In addition, the switching between shift clock signal and capture clock signal is conducted with glitch-free multiplexors (advanced techniques such as [18] is not necessary because we only need to switch between two clock signals). The virtual wrapper is connected to the core interface through internal virtual test bus (VTB) lines. To tradeoff the TAT against test power, the number of internal VTB lines ($W_{\rm vtb}$) is not necessarily the same as the external test access mechanism (TAM) width assigned to the core ($W_{\rm ext}$). Instead, bandwidth matching[2] technique [19] is utilized to map the external TAM wires to the internal VTB lines. That is, by introducing frequency converters VTB-DIU (VTB-MIU) on the input (output) of the core under test, the internal VTB lines is able to operate at a lower frequency f_s that satisfies the condition $W_{\rm ext} \times f_t \geq W_{\rm vtb} \times f_s$, where f_t is the tester frequency. It is important to note that at-speed test is controlled by on-chip high-speed clocks (e.g., from PLL) instead of the tester and, consequently, the proposed technique is particularly relevant when used in conjunction with low-speed testers. To save hardware overhead, both f_s and f_t are determined by dividing $f_{\rm TCK}$ (frequency of TCK, driven by the highest speed functional clock) by powers of 2.

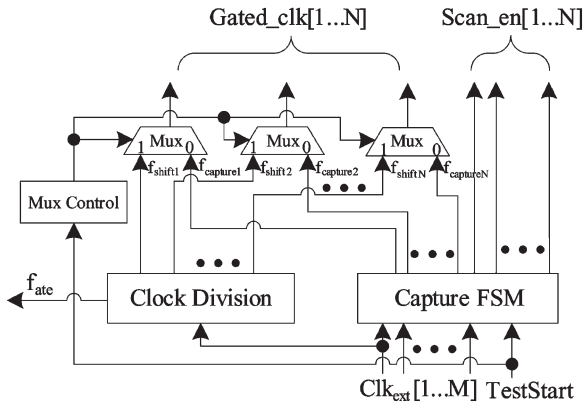

Fig. 1. Block diagram of the proposed scan control unit.

As discussed in Section I, the constraint that all the clock domains are clocked with the same signal affects the tradeoff between testing time and test power. Furthermore, by introducing a phase difference between the shift clocks used for different clock domains, the number of flip-flops that latch values at the same time can be limited to the number of flip-flops per clock domain, thus avoiding the excessive voltage drop on power/ground lines. Therefore, in this paper, we propose a power-constrained wrapper for cores with multiple clock domains. We extend the design procedure from [6] in that different clock domains can use distinct shift clock signals, which are generated inside the proposed core wrapper. This is different from the multifrequency TAM design methodologies [20], [21] proposed recently. First of all, [20] requires the tester to shift data at multiple rates. Many low- and medium-end testers are not equipped with such advanced port scalability features. The proposed power-constrained core wrapper, however, generates the distinct shift frequencies inside the core wrapper and hence allows testing even with less expensive testers. Second, the techniques proposed in [20] and [21] work at the chip level, while our solution works at the core level. Since the proposed wrapper design is transparent to the SOC-level TAM design and optimization, it can be combined with [20] and [21] when a high-end tester is available.

III. Design of Scan Control Unit

The scan control unit is a major part of the wrapper, which provides the scan enable (Scan_en) and shift/capture clock signals (Gated_clk) to all the VCs. Fig. 1 depicts the block diagram of the proposed scan control unit. As can be observed from this figure, all the M external clock signals $\mathrm{Clk}_{\rm ext}[1 \ldots M]$ (with frequencies $f_1, f_2, \ldots, f_M$[3]) that

[1]The final wrapper design is still at the core-level, and the virtual core concept is proposed mainly as a stepping stone for better understanding.

[2]Bandwidth is defined as the product of the width and the frequency of a scan architecture.

[3]Without loss of generality, we assume $f_1 > f_2 \cdots > f_M$.

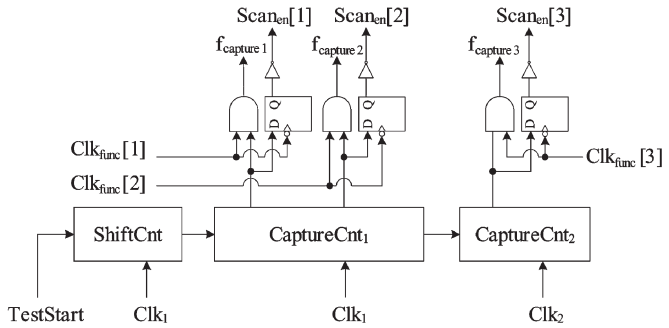

Fig. 2. Implementation of the capture FSM.

are utilized by the core internal logic feed in the scan control unit to generate the at-speed launch/capture clock pulses necessary for each clock domain. When compared to [6] in which the different VCs share the same shift clock $f_{\rm shift}$ divided from f_1, the proposed clock division unit outputs multiple shift clock signals $f_{\rm shift1}$, $f_{\rm shift2}, \ldots, f_{{\rm shift}N}$ for the N different VCs. This not only expands the solution space during wrapper optimization (as detailed in the next section), but it also decreases the instantaneous power consumption during shift by making the distinct shift clocks have a different clock phase. To simplify the hardware implementation, the ratio between f_1 and $f_{{\rm shift}i}$ for any VC i is two's exponent. Therefore, a simple shift register implementation can be used to generate these shift clock signals.

Another novel feature of the proposed scan control unit is that the scan phase is controlled solely on-chip, i.e., it does not need the external scan enable signal provided from ATE, as it is the case in the previous approach [6]. Current- and next-generation SOCs may contain tens or even hundreds of cores; hence, if the scan enable signals for all the cores are provided from the ATE, the number of pins available for test data transfer is reduced, thus increasing TAT [22]. Since the start of the test can be determined by decoding the wrapper instruction and because the length of each test pattern is known, all the scan enable signals Scan_en$[1, \ldots, N]$ can be generated internally. That is, the TestStart signal shown in Fig. 1 can be easily obtained by detecting the change of the wrapper mode to INTEST, and it functions similar to an external scan enable signal and is used to control the capture finite state machine (FSM) and the mux control unit.

The capture FSM implementation for an example multifrequency core with three clock domains (controlled by two core-external clock signals) is depicted in Fig. 2. As can be observed from the figure, the major components of this block are several counters. Counter ShiftCnt controls the transition between shift and capture phase. Its length equals the maximum shifting cycles of all the VCs. Counters CaptureCnt1 and CaptureCnt2, pulsed by external clock signals $\rm Clk_1$ and $\rm Clk_2$, respectively, are utilized to generate the predefined capture sequence in the two subcapture windows (see Fig. 3). That is, these counters generate signals that are logic "1" only in the predefined counting sequence for each VC, which are then "ANDed" with each VC's functional clock to generate the capture clock signals and at the same time feed into negative-edge triggered flip-flops to generate the appropriate scan enable signals.

Fig. 3 compares the timing diagram of the proposed methodology and the one in [6]. We can easily observe the difference between the scan shift frequencies and phases. The frequency of Gated_clk [3] is half of the frequencies of Gated_clk [1] and Gated_clk [2] in Fig. 3(b). In addition, although the shift frequencies of Gated_clk [1] and Gated_clk [2] are the same, their clock phases are opposite in order to reduce instantaneous test power. We can also see the capture window designs are the same for Fig. 3(a) and (b), in which multiple capture cycles are utilized to avoid clock skew in scan capture phase. It can be observed that the paths that cross clock domains are also tested (not at-speed, though) because the earlier-captured domains pass the data to the later-captured domains in the capture window. Advanced ATPG techniques, as described in [23] and [24], are assumed to be used for such situation.

For the design for testability (DFT) cost of the proposed wrapper design, the capture window size and the number of clock domains decide the hardware overhead of the scan control unit, which is similar to the one that was reported in [6]. For example, for a representative multifrequency core hCADT00 [6], the increased DFT area is less than 400 gates. This is a small fraction of the area of the IEEE Std. 1500 wrapper and scan logic, which together add over 4000 gates. For today's complex cores with hundreds of thousands of gates, the aforementioned DFT cost is insignificant, especially considering the benefit of at-speed multifrequency test of IP-protected cores.

IV. Wrapper Optimization

Recall that the new scan control design enables the scan chains for different clock domains to shift data at distinct frequencies, thereby reducing TAT under power constraints. In this section, we propose a new wrapper optimization procedure to determine the different shift frequencies and minimize TAT. The problem can be stated as follows.

Problem $P_{\rm mfw\text{-}opt}$: Given the test set parameters for the multifrequency core, including: 1) the number of clock domains $N_{\rm c}$; 2) for each clock domain (VC) i, the number of primary inputs $N_{\rm in}$, primary outputs $N_{\rm out}$, and bidirectional I/Os $N_{\rm bi}$, the number of scan chains $N_{\rm sc}$ and scan chain lengths for fixed-length scan chains $\rm SC_{length,\it i}$ (or the number of scan cells when scan chains are flexible $N_{\rm ff}$); the number of test patterns N_P and the average power consumption P_i when it is shifted at the minimum allowed frequency F_M (discussed in Section IV-A); 3) the maximum allowed average test power $P_{\rm ave}$; 4) the ATE shift frequency f_t; and 5) the external TAM width $W_{\rm ext}$, determine the wrapper design for the core, including: a) the shift frequency $f_{{\rm shift}i}$ for each clock domain i, $1 \le i \le N_{\rm c}$; b) the number of VTB lines W_i for each clock domain i, $1 \le i \le N_{\rm c}$; and c) the WSC design, such that the TAT of the core $T_{\rm core}$ is minimized and the internal scan bandwidth matches the external scan bandwidth. As $T_{\rm core}$ is the product of the given test pattern count N_P and the testing time for each test pattern $T_{\rm pattern}$, we simply consider reducing $T_{\rm pattern}$ during the wrapper optimization process.

In this section, we first develop an ILP model for $P_{\rm mfw\text{-}opt}$ problem. Due to the high computational cost of the ILP method, we also introduce an efficient heuristic to solve this problem. Despite its computational complexity, the ILP model is not only useful to generate optimal solutions for small problem instances with limited number of clock domains (e.g., $N_{\rm c} \le 3$), but it is also essential for us to evaluate the effectiveness of the proposed heuristic for large problem instances by comparing these exact solutions to the heuristic solutions. In addition, the computation time for the ILP model can be reduced by LP-relaxation, whereby some carefully chosen integer variables are allowed to take noninteger values. This results in useful lower bounds on the testing time, as presented in Section V.

A. Wrapper Optimization Using An ILP Model

Suppose the possible shift frequencies for each VC are $f_{{\rm shift}i} \in \{F_1, F_2, \ldots, F_M\}$, which satisfy: 1) $F_{k+1} = F_k/2, k \in \{1, 2, \ldots, M-1\}$ (the "divided by a power of 2" relationship guarantees easy hardware implementation) and 2) $F_1 \times 1 + F_M \times (N_{\rm c} - 1) \le f_t \times W_{\rm ext}$, i.e., the external scan bandwidth exceeds the internal bandwidth when the number of VTB lines for every VC is 1 and one clock domain shifts at F_1, while all the other clock domains shift at

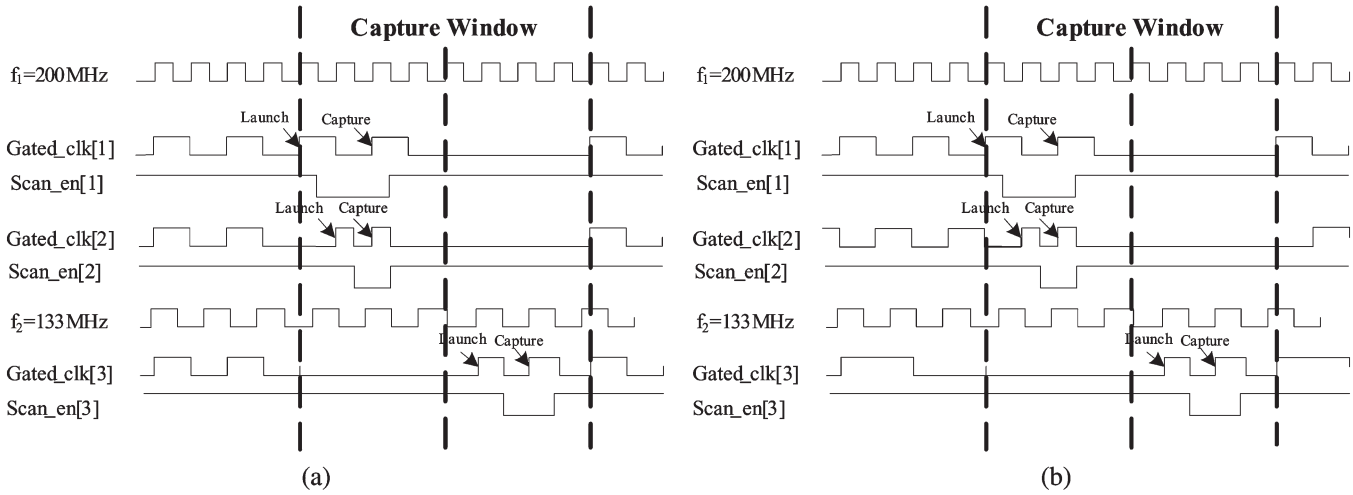

Fig. 3. Comparison of timing diagrams. (a) Timing diagram of the architecture with common shift clock [6]. (b) Timing diagram of the proposed architecture with distinct shift clocks.

F_M. Hence, when the number of possible frequencies M is given (we assume $M = 4$ in this paper), the values of $F_1, \ldots, F_M$ can be predetermined based on the above constraints.

Let W_i denote the number of VTB lines assigned to clock domain i. Now, the maximum possible value of W_i is $W_{\max} = (f_t/f_M) \times W_{\text{ext}} - N_c + 1$. We are able to precalculate $T_i(F_k, j)$, which is the TAT for each test pattern for clock domain i, when W_i is equal to j and $f_{\text{shift}i}$ is equal to F_k. Let us define the binary variable δ_{ij} as $\delta_{ij} = 1$ only if $W_i = j$, where $j \in \{1, 2, \ldots, W_{\max}\}$. In addition, let us define the binary variable θ_{ik} as $\theta_{ik} = 1$ only if domain i is given a shift frequency F_k, where $k \in \{1, 2, \ldots, M\}$. Then, the TAT for each test pattern is

$$T_{\text{pattern}} = \max_i \left\{ \sum_{j=1}^{W_{\max}} \sum_{k=1}^{M} \delta_{ij}\theta_{ik}T_i(F_k, j) \right\}. \quad (1)$$

The following constraints must be satisfied as follows.

1) $\sum_{j=1}^{W_{\max}} \delta_{ij} = 1,\ 1 \le i \le N_c$, i.e., every VC is assigned to exactly one VTB.
2) $\sum_{k=1}^{M} \theta_{ik} = 1,\ 1 \le i \le N_c$, i.e., test patterns for a VCs are shifted at exactly one frequency.
3) $\sum_{i=1}^{N_c} \sum_{k=1}^{M} \theta_{ik} \times P_i \times (F_k/F_M) \le P_{\text{ave}}$, i.e., the power rating is not exceeded.
4) $\sum_{i=1}^{N_c} W_i \times f_{\text{shift}i} \le W_{\text{ext}} \times f_t$, i.e., the external scan bandwidth is not exceeded.

Since we have

$$W_i = \sum_{j=1}^{W_{\max}} \delta_{ij} \times j \quad (2)$$

$$f_{\text{shift}i} = \sum_{k=1}^{M} \theta_{ik}F_k = \sum_{k=1}^{M} \theta_{ik}2^{M-k}F_M. \quad (3)$$

Constraint 4) can be converted to

$$\sum_{i=1}^{N_c} \sum_{j=1}^{W_{\max}} \sum_{k=1}^{M} 2^{M-k}\delta_{ij}\theta_{ik}j \le W_{\text{ext}} \times \left(\frac{f_t}{F_M}\right). \quad (4)$$

The nonlinear term $\delta_{ij}\theta_{ik}$, must be linearized so that we use linear programming tools to solve this problem. This is done by introducing a new binary variable $\lambda_{ijk} = \delta_{ij}\theta_{ik}$ with additional constraints, which yields the following ILP model.

Objective: Minimize $\max_i\{\sum_{j=1}^{W_{\max}} \sum_{k=1}^{M} \lambda_{ijk}T_i(F_k, j)\}$, subject to the following constraints:

1) $\sum_{j=1}^{W_i^{\max}} \delta_{ij} = 1, \quad 1 \le i \le N_c$;
2) $\sum_{k=1}^{M} \theta_{ik} = 1, \quad 1 \le i \le N_c$;
3) $\sum_{i=1}^{N_c} \sum_{k=1}^{M} 2^{M-k}\theta_{ik}P_i \le P_{\text{ave}}$;
4) $\sum_{i=1}^{N_c} \sum_{j=1}^{W_{\max}} \sum_{k=1}^{M} 2^{M-k}\lambda_{ijk}j \le W_{\text{ext}} \times (f_t/F_M)$;
5) $\delta_{ij} + \theta_{ik} - \lambda_{ijk} \le 1, 1 \le i \le N_c, 1 \le j \le W_{\max}, 1 \le k \le M$;
6) $\delta_{ij} + \theta_{ik} - 2\lambda_{ijk} \ge 0, 1 \le i \le N_c, 1 \le j \le W_{\max}, 1 \le k \le M$.

It should be noted that with the binary attribute of δ_{ij}, θ_{ik} and λ_{ijk}, constraints 5) and 6) above effectively ensure that $\lambda_{ijk} = \delta_{ij}\theta_{ik}$. For example, when $\delta_{ij} = 0$, the constraint 6) becomes $\theta_{ik} - 2\lambda_{ijk} \ge 0$ and hence $\lambda_{ijk} = 0$. When $\delta_{ij} = 1$, if $\theta_{ik} = 1$, the constraint 5) requires $\lambda_{ijk} = 1$; if $\theta_{ik} = 0$, the constraint 6) guarantees $\lambda_{ijk} = 0$. As a result, $\lambda_{ijk} = \theta_{ik}$ when $\delta_{ij} = 1$, which is appropriate.

The number of variables Num_v and constraints Num_c for this ILP model are $N_cW_{\max} + N_cM + N_c\text{MW}_{\max}$ and $2N_c\text{MW}_{\max} + 2N_c + 2$, respectively. Since Num_v and Num_c can easily be in the range of thousands for a core with large values for N_c and/or W_{ext}, using an ILP solver to obtain the optimal TAM configuration requires large computation time. Before introducing an efficient heuristic for problem $P_{\text{mfw-opt}}$ in the next section, we show how lower bounds on the TAT can be obtained using LP-relaxation. Here, the variables θ_{ik}, hence also λ_{ijk} in the ILP model are "relaxed" to reals. This relaxation does not affect constraints 5) and 6). When the binary variable $\delta_{ij} = 0$, $\theta_{ik} - 1 \le \lambda_{ijk} \le \theta_{ik}/2$. Since the objective function of the ILP model can be also seen as to minimize λ_{ijk} and $\lambda_{ijk} \ge 0$, λ_{ijk} is assigned the value 0 and it is consistent with $\lambda_{ijk} = \delta_{ij}\theta_{ik}$. When $\delta_{ij} = 1$, $\theta_{ik} \le \lambda_{ijk} \le (\theta_{ik} + 1)/2$. Again, to minimize λ_{ijk}, it is assigned the value θ_{ik}, which is also appropriate. It is important to note that, due to the nature of LP-relaxation, these lower bounds are not "tight," which implies that they may not be achievable in practice. Nevertheless, they provide useful insights into the quality of heuristic solutions, especially for large problem instances, for which optimal solutions using the ILP model may not be easily available.

B. Heuristic for Wrapper Optimization

The algorithm for core wrapper design with multiple shift frequencies (CWDMSF) takes as inputs the tester frequency (f_t), the test

Algorithm 1: *CWDMSF*

INPUT: C, W_{ext}, f_t, N_c, *NoWeights*, $\{F_1,...,F_M\}$, P_{ave}
OUTPUT: f_{shifti}, $VC=\{VC^i|i=1...N_c\}$

1. Initialize VC;
2. $N_{vtb}=W_{ext}\times\frac{f_t}{F_M}$; $N_{assigned\_vtb}=0$;
3. $P_{curr}=\sum_{i=1}^{N_c}P_i$;
4. **if**($P_{curr}>P_{ave}$) **exit**;
. /*First assign every VC 1-bit VTB line*/
5. **for** i from 1 to N_c {
6. $f_{shifti}=F_M$; $VTB_{vc^i}=1$;
7. $N_{assigned\_vtb}$++;
8. **do** SFCWD;
. }
. /*Wrapper optimization with different power weight*/
9. **for** *powerWeight* from 0 to $NoWeights-1$ {
10. **while** ($N_{vtb}>N_{assigned\_vtb}$) {
11. find VC^g with TAT $\tau_g=\max\{\tau_i\}$ for all VCs;
12. copy VC^g to VC^{temp};
13. $N_{temp}=N_{assigned\_vtb}$;
14. compute P_{curr};
15. $AssignVTBtoVC(VC^{temp},P_{curr},P_{ave},N_{vtb},N_{temp},powerWeight)$;
16. **if** ($\tau_{temp}<\tau_g$) {
17. copy VC^{temp} to VC^g;
18. $N_{assigned\_vtb}=N_{temp}$;
. } **else** {
19. **break**; }
. }
20. $T_{shift}=\max\{\tau_i\}$ for all VCs;
21. record the VC design with the minimum T_{shift};
. }
22. **return** f_{shifti}, VC;

Fig. 4. Pseudocode for wrapper design with multiple shift frequencies.

Algorithm 2: *AssignVTBtoVC*

INPUT: VC^{temp}, P_{curr}, P_{ave}, N_{temp}, N_{vtb}, *powerWeight*
OUTPUT: τ_{temp}, f_{temp}, $VTB_{VC^{temp}}$, N_{temp}

1. $\tau_{orig}=\tau_{temp}$;
2. $P_{orig}=P_{temp}$; $P_{others}=P_{curr}-P_{orig}$;
3. **while** (($\tau_{temp}\geq\tau_{orig}$) && ($N_{vtb}>N_{temp}$)) {
4. $f_{temp}=F_M$; $VTB_{VC^{temp}}=VTB_{VC^{temp}}\times\frac{f_{temp}}{F_M}$;
5. $VTB_{VC^{temp}}$++; N_{temp}++;
6. $noTrials=M$;
7. $minCost=\infty$;
. /*Find the shift frequency with the minimum cost*/
8. **while** ($--noTrials>0$) {
9. **do** SFCWD;
10. compute τ_{temp}, P_{temp};
. /*Build the cost function*/
11. $currCost=(\tau_{temp}-\tau_{orig})+\frac{powerWeight}{normalWeight}\times(P_{temp}-P_{orig})$;
12. **if** ($\tau_{temp}<\tau_{orig}$ && $currCost<=minCost$) {
13. $minCost=currCost$;
14. record the current virtual core wrapper design; }
15. **if** ($VTB_{VC^{temp}}\%2==0$ && $P_{others}+2P_{temp}<=P_{ave}$) {
16. $f_{temp}=f_{temp}\times2$;
17. $VTB_{VC^{temp}}=VTB_{VC^{temp}}\div2$;
18. } **else** {
19. **break**; }
. }
. }
20. **return** τ_{temp}, f_{temp}, $VTB_{VC^{temp}}$, N_{temp};

Fig. 5. Procedure for assigning VTB lines to the bottleneck VC.

parameters of the multifrequency core (C), the TAM width $(W_{\rm ext})$, the predetermined possible shift frequency $\{F_1,\ldots,F_M\}$, the number of clock domains $N_{\rm c}$, and the maximum test power consumption $P_{\rm ave}$. It outputs the wrapper design VC, including the shift frequency $f_{{\rm shift}i}$ and the number of VTB lines $\mathrm{VTB}_{\mathrm{VC}^i}$, for each VC VC^i. The pseudocode for this procedure is shown in Fig. 4.

The algorithm initializes the VCs, by assigning to each VC the inputs, the scan chains and the outputs which operate in its clock domain (line 1). In line 2, all the VTB lines are initialized to operate at the lowest possible frequency F_M. Line 3 computes the power consumption $P_{\rm curr}$ (at this moment P_i is the power consumption for clock domain i when shifted at F_M) and if $P_{\rm curr}>P_{\rm ave}$ then the program exits because it cannot satisfy the power constraint (line 4). Otherwise, each VC VC^i is first allocated with one VTB line and then single-frequency core wrapper design (SFCWD) is performed (Design_wrapper [25]) to get an initial testing time (lines 5–8) as the starting point for VTB line allocation (lines 9–21).

Depending on $N_{\rm vtb}$, the algorithm proceeds as follows. First, all the VCs are sorted based on their TAT and the bottleneck VC (with longest TAT) is identified (line 11). Then, the following steps iteratively assign the remaining VTB lines to VCs. The basic idea is to assign more VTB lines to the bottleneck VC. This greedy strategy is similar to the algorithm proposed in [26] for distributed scan chain architecture. However, the main difference lies in the fact that not only we try different possible shift frequencies when assigning VTB lines, but also more importantly, we take both test power and testing time into account during the optimization process. This is because, although increasing the frequency will lower TAT, if the current bottleneck VC is assigned a higher frequency without considering the increase in power, a suboptimal solution may be obtained because the available power budget for the next iteration is reduced. To account for this problem, we build a cost function that combines TAT and power, and we select the shift frequency that can obtain the minimum cost instead of minimum TAT. This is done in Algorithm 2 (Fig. 5), which assigns VTB lines to the bottleneck VC. NoWeights number of power weights in the cost function are tried and we select the one which gives the shortest TAT (line 21).

Algorithm 2 is a greedy heuristic that assigns one VTB line operating at F_M to the bottleneck VC each time. To apply this, the bottleneck VC is first transformed to a temporary VC which operates at F_M (line 4). Inside the inner loop (lines 8–19), the algorithm selects the shift frequency that minimize the cost and at the same time satisfies the power constraint (lines 12, 15). The cost function is built as in line 11, in which normalWeight is a constant used to match the TAT and the power consumption into comparable values. In our experiments, we select NoWeights $=100$ and normalWeight $=200$ to limit the run time to a few seconds. Whenever a VTB line is assigned, SFCWD is performed again to get the new testing time (line 9). This procedure exits when the TAT of the bottleneck VC is reduced or all the VTB lines are assigned with no TAT reduction.

The worst case complexity of the single frequency wrapper design algorithm Design_wrapper is shown to be $O(\mathrm{sc}\cdot\log\mathrm{sc}+\mathrm{sc}\cdot W_{\rm ext})$ in [25], where sc is the number of internal scan chains. The worst case complexity of the proposed CWDMSF algorithm is $O(\sum_{i=1}^{N_{\rm c}}\mathrm{sc}_i\cdot\log\mathrm{sc}_i+W_{\rm ext}\cdot\mathrm{sc}_{\max}\cdot\log\mathrm{sc}_{\max}+W_{\rm ext}^2\cdot\mathrm{sc}_{\max})$, where sc_i and $\mathrm{sc}_{\max}$ are the number of internal scan chains for clock domain i and the maximum number of scan chains of all clock domains, respectively. The computational complexity is therefore linear in the number of clock domains and quadratic in the number of external TAM wires.

V. Experimental Results

To illustrate the importance of employing multiple shift frequencies in the wrapper architecture, this section shows the comparison between

TABLE I
hCADT01 CLOCK DOMAIN INFORMATION

I_c	N_{in}	N_{out}	N_{bi}	P	N_{sc}	$SC_{length,\ i}$
1	109	32	72	2572	16	{168 168 166 166 163 163 163 163 162 162 162 162 151 151 151 151}
2	144	67	72	450	3	{150 150 150}
3	89	8	72	930	10	{93 93 93 93 93 93 93 93 93 93}
4	111	31	72	1314	6	{219 219 219 219 219 219}
5	117	224	72	2605	5	{521 521 521 521 521}
6	146	68	72	576	11	{82 82 82 81 81 81 18 18 17 17 17}
7	15	30	72	40	4	{10 10 10 10}

TABLE II
hCADT02 CLOCK DOMAIN INFORMATION

I_c	N_{in}	N_{out}	N_{bi}	P	N_{sc}	$SC_{length,\ i}$
1	79	32	32	10350	30	{345 345 ... 345}
2	44	47	32	7040	22	{320 320 ... 320}
3	40	14	0	15000	50	{300 300 ... 300}
4	33	31	32	2400	8	{300 300 ... 300}
5	17	18	0	1800	6	{300 300 ... 300}
6	30	56	32	1500	5	{300 300 ... 300}
7	14	20	0	480	2	{240 240}
8	16	18	32	200	1	{200}

the wrapper design algorithm proposed in this paper and the one based on a single shift frequency reported in [6]. Benchmark SOCs available in the public domain do not contain clock domain information about the embedded cores. Detailed information about cores with multiple clock domains is also not available from industry. The hTCADT00 core used in [6] does not have a large number of clock domains and flip-flops. In order to show the TAT variations under power constraints, we have constructed two complex multifrequency cores. The first core hCADT01 is created based on cores from ITC'02 SOC benchmark set [27], while hCADT02 is constructed based on the information available for the Samsung multifrequency microprocessor core Y presented in [28]. The two cores have seven and eight clock domains, respectively, as shown in Tables I and II, respectively. $I_{\rm c}$ denotes the index of each clock domain; $N_{\rm in}$, $N_{\rm out}$, $N_{\rm bi}$, and $N_{\rm sc}$ are the number of inputs, outputs, bidirectionals, and scan chains in the specific clock domain, respectively; the length of each scan chain in clock domain i is shown in column $\mathrm{SC}_{\mathrm{length},i}$ (the lengths "..." for scan chains in the first six-clock domains of hCADT02 denote they are the same as the value before and after it); and P is the average power consumption when test data is shifted at 100 MHz.[4] It can be easily observed that the internal scan chains are unbalanced in hCADT01, while they are quite balanced in hCADT02. In the absence of a given power consumption profile for a core, we assume that the power consumption of a VC is proportional to the number of memory elements in it and the test power is simply calculated as $P_i = \sum_{j=1}^{|\mathrm{SC}_{\mathrm{length},i}|}(l_j|l_j \in \mathrm{SC}_{\mathrm{length},i})$. In practice, power profiling or data on power consumption can be used to parameterize the test power in terms of the number of scan elements, the number of scan chains, and the shift frequency.

Tables III and IV compare the shifting time per test pattern for multifrequency cores hCADT01 and hCADT02 when different power constraints $P_{\rm ave}$ are considered. $T_{[6]}$ denotes the TAT for the single frequency shift architecture from [6] and $T_{\rm new}$ stands for the TAT obtained by the multifrequency shift architecture from this paper derived using the heuristic approach from Section IV-B. ΔT is computed as $\Delta T = (T_{\rm new} - T_{[6]})/(T_{[6]})$. For both cores, even when there is no power constraint (i.e., $P_{\rm ave} = \infty$), we can observe that the shifting time is reduced for almost all the given TAM widths. For hCADT01, we can also observe that the proposed architecture leads to much shorter TAT when the power constraint is tighter. For example, when the given TAM width is $W_{\rm ext} \geq 6$ and the power constraint $P_{\rm ave} = 1500$, $T_{\rm new}$ is only half of $T_{[6]}$. This is because all the VCs are constrained to shift at 12.5 MHz to meet the power requirements in the single-frequency shift architecture from [6], and clock domain 5 dominates with TAT $= 41.68$ μs. With the architecture proposed in this paper, clock domain 5 is able to shift at 25 MHz which results in TAT $= 20.84$ μs, while still meeting the power constraint. For hCADT02, it can be observed the savings in testing time are about 10% on average, which is rather limited when compared to the savings for hCADT01. This is mainly because, when the internal scan chains are balanced for each VC, there is a high possibility that the WSCs constructed by stitching these internal scan chains and wrapper boundary cells together in each VC are also balanced. In other words, the WSC length of the bottleneck VC is similar to the one of the other VCs. Therefore, even if we are able to increase the shift frequency of the bottleneck VC without exceeding power constraint, the test length of the new bottleneck VC is similar to the original one and hence the testing time cannot be significantly reduced. We have also implemented the ILP method using a public-domain linear programming solver lp_solve for both hCADT01 and hCADT02 [29]. We obtain the same results as the heuristic method when $W_{\rm ext} \leq 4$. When the external TAM width is larger, lp_solve does not run to completion in 10 hours, using a 900-MHz Pentium III PC with 256-MB memory. The execution time of the heuristic is, however, only a few seconds. Nevertheless, the ILP method is useful because it shows that the heuristic yields optimal results for $W_{\rm ext} \leq 4$. In addition, for $W_{\rm ext} > 4$, the lower bounds are obtained using LP-relaxation, as discussed in Section IV-A. The lower bounds for both $W_{\rm ext} \leq 4$ (obtained through ILP) and $W_{\rm ext} > 4$ (from LP-relaxation), are shown in columns $T_{\rm lb}$ of Tables III and IV, from which we can observe that the proposed heuristics generate values close to them. What is interesting to note is that hCADT01 and hCADT02 show two opposite corners of the solution space. On the one hand, if the scan chain lengths are balanced, the benefits of the proposed solution are rather limited, but we are still able to achieve about 10% improvement. On the other hand, if the scan chain lengths are unbalanced, then the test time savings are significant, especially under tight power constraints.

In this paper, we mainly consider the case when all VCs are tested concurrently and we calculate the lower bound for the shifting time for each test pattern accordingly. In Tables V and VI, however, we compare $T_{\rm new}$ with the case when all VCs are sequentially tested ($T_{\rm r}$). It can be observed that on average we can achieve 16% and 36% reduction in shifting time for each test pattern for hCADT01 and hCADT02, respectively. It is important to note that because in our proposed method the multiple clock domains are captured in sequence in the capture window, the number of required test patterns is usually much less than the scenario where each clock domain is tested sequentially [3]. Therefore, even for the few cases where the proposed method results in longer loading time per pattern, the actual time that accounts for all the test patterns will be lower. In addition, the logic that crosses between multiple clock domains is implicitly tested in the proposed method, while for the case when all VCs are tested sequentially, dedicated test needs to be done, which also adds to the overall testing time.

It is also interesting to point out that our test power reduction approach (i.e., assigning shift frequency for each clock domain intelligently to meet the power constraint) is compatible with low-power scan techniques. For example, suppose we apply the low-power scan architecture proposed in [30], which is based on scan chain segmentation and has been widely adopted in practice for handling the shift power. We can assume that we transform every original scan

[4]We assume ATE operates at $f_t = 100$ MHz in our experiments.

TABLE III
COMPARISON OF SHIFTING TIME PER TEST PATTERN FOR hCADT01 WITH [6]

	$P_{ave}=1500$				$P_{ave}=3000$				$P_{ave}=4500$				$P_{ave}=\infty$			
W_{ext}	T_{lb}	$T_{[6]}$	T_{new}	$\Delta T(\%)$	T_{lb}	$T_{[6]}$	T_{new}	$\Delta T(\%)$	T_{lb}	$T_{[6]}$	T_{new}	$\Delta T(\%)$	T_{lb}	$T_{[6]}$	T_{new}	$\Delta T(\%)$
24	20.84	41.68	20.84	-50	10.42	20.84	10.42	-50	6.72	10.42	6.72	-35.51	5.21	5.21	5.21	0
23	20.84	41.68	20.84	-50	10.42	20.84	10.42	-50	6.72	10.42	6.72	-35.51	5.21	5.21	5.21	0
22	20.84	41.68	20.84	-50	10.42	20.84	10.42	-50	6.72	10.42	6.72	-35.51	5.21	5.46	5.21	-4.58
21	20.84	41.68	20.84	-50	10.42	20.84	10.42	-50	6.72	10.42	6.72	-35.51	5.21	5.81	5.3	-8.78
20	20.84	41.68	20.84	-50	10.42	20.84	10.42	-50	6.72	10.42	6.72	-35.51	5.21	6.39	5.81	-9.08
19	20.84	41.68	20.84	-50	10.42	20.84	10.42	-50	6.72	10.42	6.72	-35.51	5.4	6.66	6	-9.91
18	20.84	41.68	20.84	-50	10.42	20.84	10.42	-50	6.72	10.42	6.72	-35.51	5.66	6.89	6.39	-7.26
17	20.84	41.68	20.84	-50	10.42	20.84	10.42	-50	6.72	10.42	6.92	-33.59	6	7.49	6.66	-11.08
16	20.84	41.68	20.84	-50	10.42	20.84	10.42	-50	6.72	10.42	7.44	-28.60	6.4	7.94	7.44	-6.30
15	20.84	41.68	20.84	-50	10.42	20.84	10.42	-50	6.91	10.42	8.76	-15.93	6.8	9.59	7.49	-21.90
14	20.84	41.68	20.84	-50	10.42	20.84	10.42	-50	7.51	10.42	8.88	-14.80	7.33	10.42	8.88	-14.78
13	20.84	41.68	20.84	-50	10.42	20.84	10.42	-50	8.17	10.42	10.42	0	7.99	10.42	9.59	-7.97
12	20.84	41.68	20.84	-50	10.42	20.84	10.42	-50	8.79	10.42	10.42	0	8.73	10.42	10.42	0
11	20.84	41.68	20.84	-50	10.42	20.84	11.62	-44.24	9.62	10.92	10.42	-4.58	9.44	10.92	10.42	-4.58
10	20.84	41.68	20.84	-50	10.51	20.84	12.08	-42.03	10.42	12.78	11.62	-9.08	10.33	12.78	11.62	-9.08
9	20.84	41.68	20.84	-50	11.51	20.84	13	-37.62	11.33	13.78	12.78	-7.26	11.33	13.78	12.78	-7.26
8	20.84	41.68	20.84	-50	12.93	20.84	14.48	-30.52	12.82	15.88	14.88	-6.30	12.81	15.88	14.88	-6.30
7	20.84	41.68	20.84	-50	14.73	20.84	17.76	-14.78	14.73	20.84	15.63	-25	14.73	20.84	15.63	-25
6	20.84	41.68	20.84	-50	17.52	20.84	20.84	0	17.52	20.84	19.2	-7.87	17.52	20.84	19.18	-7.97
5	21.24	41.68	25.04	-39.92	20.85	25.56	23.24	-9.08	20.85	25.56	23.24	-9.08	20.85	25.56	23.24	-9.08
4	29.76	41.68	29.76	-28.60	29.76	31.76	29.76	-6.30	29.01	31.76	29.01	-8.66	29.01	31.76	29.01	-8.66
3	41.68	41.68	41.68	0	38.36	41.68	38.36	-7.97	38.36	41.68	38.36	-7.97	38.36	41.68	38.36	-7.97
2	59.88	63.52	59.88	-5.73	58.02	63.52	58.02	-8.66	58.02	63.52	58.02	-8.66	58.02	63.52	58.02	-8.66
1	116.04	127.04	116.04	-8.66	116.04	127.04	116.04	-8.66	116.04	127.04	116.04	-8.66	116.04	127.04	116.04	-8.66

TABLE IV
COMPARISON OF SHIFTING TIME PER TEST PATTERN FOR hCADT02 WITH [6]

	$P_{ave}=4000$				$P_{ave}=8000$				$P_{ave}=12000$				$P_{ave}=\infty$			
W_{ext}	T_{lb}	$T_{[6]}$	T_{new}	$\Delta T(\%)$	T_{lb}	$T_{[6]}$	T_{new}	$\Delta T(\%)$	T_{lb}	$T_{[6]}$	T_{new}	$\Delta T(\%)$	T_{lb}	$T_{[6]}$	T_{new}	$\Delta T(\%)$
32	48	55.2	48	-13.04	24	27.6	24	-13.04	13.8	13.8	13.8	0	12.62	13.8	13.8	0
31	48	55.2	48	-13.04	24	27.6	24	-13.04	13.8	13.96	13.96	0	13.06	13.96	13.96	0
30	48	55.2	48	-13.04	24	27.6	24	-13.04	13.8	24	18.18	-24.25	13.51	16	15	-6.25
29	48	55.2	48	-13.04	24	27.6	24	-13.04	14.21	24	19.2	-20	13.91	17.25	15.04	-12.81
28	48	55.2	48	-13.04	24	27.6	24	-13.04	15.01	24	24	0	14.44	17.44	16	-8.26
27	48	55.2	48	-13.04	24	27.6	24	-13.04	15.76	24	24	0	14.97	18	17.44	-3.11
26	48	55.2	48	-13.04	24	27.6	24	-13.04	16.57	24	24	0	15.72	18.18	18	-0.99
25	48	55.2	48	-13.04	24	27.6	24	-13.04	17.35	24	24	0	16.5	19.2	18	-6.25
24	48	55.2	48	-13.04	24	27.6	24	-13.04	18.13	24	24	0	17.1	20.7	18.18	-12.17
23	48	55.2	48	-13.04	24	27.6	24	-13.04	18.93	24	24	0	17.74	20.7	19.2	-7.25
22	48	55.2	48	-13.04	24	27.6	25.44	-7.83	19.78	25.6	24	-6.25	18.58	20.94	20.7	-1.15
21	48	55.2	48	-13.04	24	27.6	25.6	-7.25	20.68	25.6	24	-6.25	19.56	24	21	-12.50
20	48	55.2	48	-13.04	24	27.6	25.6	-7.25	21.57	25.6	24	-6.25	20.62	24	24	0
19	48	55.2	48	-13.04	24	27.6	27.6	0	22.45	25.6	24	-6.25	21.82	25.6	24	-6.25
18	48	55.2	48	-13.04	24	27.6	27.6	0	23.29	27.6	25.44	-7.83	22.97	27.6	25.44	-7.83
17	48	55.2	48	-13.04	24.16	27.6	27.6	0	24	27.6	25.6	-7.25	23.9	27.6	25.6	-7.25
16	48	55.2	48	-13.04	25.46	27.6	27.6	0	25.25	27.6	27.6	0	25.24	27.6	27.6	0
15	48	55.2	48	-13.04	27.25	48	36.36	-24.25	27.04	36	34.5	-4.17	27.03	32	30	-6.25
14	48	55.2	48	-13.04	29.38	48	40	-16.67	28.92	36	36	0	28.88	34.88	32	-8.26
13	48	55.2	48	-13.04	32.15	48	41.4	-13.75	31.77	36.36	36	-0.99	31.34	36.36	35.6	-2.09
12	48	55.2	48	-13.04	34.98	48	48	0	34.26	41.4	40	-3.38	33.88	41.4	36	-13.04
11	48	55.2	50.88	-7.83	38.38	51.2	48	-6.25	37.19	41.88	41.4	-1.15	36.66	41.88	40	-4.49
10	48	55.2	51.2	-7.25	41.58	51.2	48	-6.25	41.24	48	48	0	41.02	48	48	0
9	48	55.2	55.2	0	45.94	55.2	50.88	-7.83	45.94	55.2	50.88	-7.83	45.94	55.2	50.88	-7.83
8	50.92	55	55.2	0	50.49	55.2	55.2	0	50.49	55.2	55.2	0	50.1	55.2	52.31	-5.24
7	58.77	96	80	-16.67	57.76	72	71.2	-1.11	57.76	69.76	64	-8.26	57.76	69.76	64	-8.26
6	70.09	96	96	0	68.4	82.8	72.72	-12.17	67.98	82.8	72	-13.04	67.85	82.8	72	-13.04
5	84.57	102.4	96	-6.25	82.73	96	96	0	82.63	96	96	0	82.58	96	96	0
4	110.4	110.4	110.4	0	110.4	110.4	110.4	0	110.4	110.4	110.4	0	104.61	110.4	104.61	-5.24
3	145.44	165.6	145.44	-12.17	144	165.6	144	-13.04	144	165.6	144	-13.04	144	165.6	144	-13.04
2	240.64	240.64	240.64	0	240.64	240.64	240.64	0	240.64	240.64	240.64	0	240.64	240.64	240.64	0.
1	481.28	481.28	481.28	0	481.28	481.28	481.28	0	481.28	481.28	481.28	0	481.28	481.28	481.28	0

chain in the multifrequency cores hCADT01 and hCADT02 into three scan segments. Given the correlation between the scan shift power and CUT power, we consider that every VC consumes 1/3 of the original test power shown in Tables I and II. Hence, for core hCADT01 when $P_{\text{ave}}=1500$, when using three scan segments and the technique in [6], its testing time is the same as the testing time for the original

TABLE V
COMPARISON OF SHIFTING TIME PER TEST PATTERN FOR hCADT01 WITH SEQUENTIAL TESTING

	$P_{ave} = 1500$			$P_{ave} = 3000$			$P_{ave} = 4500$			$P_{ave} = \infty$		
W_{ext}	T_r	T_{new}	$\Delta T(\%)$	T_r	T_{new}	$\Delta T(\%)$	T_r	T_{new}	$\Delta T(\%)$	T_r	T_{new}	$\Delta T(\%)$
24	19.32	20.84	7.87	12.43	10.42	-16.17	12.43	6.72	-45.94	12.43	5.21	-58.09
23	19.32	20.84	7.87	12.43	10.42	-16.17	12.43	6.72	-45.94	12.43	5.21	-58.09
22	19.32	20.84	7.87	12.43	10.42	-16.17	12.43	6.72	-45.94	12.43	5.21	-58.09
21	19.32	20.84	7.87	12.43	10.42	-16.17	12.43	6.72	-45.94	12.43	5.3	-57.36
20	19.32	20.84	7.87	12.43	10.42	-16.17	12.43	6.72	-45.94	12.43	5.81	-53.26
19	19.32	20.84	7.87	12.43	10.42	-16.17	12.43	6.72	-45.94	12.43	6	-51.73
18	19.32	20.84	7.87	12.43	10.42	-16.17	12.43	6.72	-45.94	12.43	6.39	-48.59
17	19.32	20.84	7.87	12.43	10.42	-16.17	12.43	6.92	-44.33	12.43	6.66	-46.42
16	19.42	20.84	7.31	12.48	10.42	-16.51	12.48	7.44	-40.38	12.48	7.44	-40.38
15	22	20.84	-5.27	13.77	10.42	-24.33	13.77	8.76	-36.38	13.77	7.49	-45.61
14	22.01	20.84	-5.32	13.78	10.42	-24.38	13.78	8.88	-35.56	13.78	8.88	-35.56
13	22.23	20.84	-6.25	13.89	10.42	-24.98	13.89	10.42	-24.98	13.89	9.59	-30.96
12	22.24	20.84	-6.29	13.9	10.42	-25.04	13.9	10.42	-25.04	13.9	10.42	-25.04
11	22.56	20.84	-7.62	14.1	11.62	-17.59	14.1	10.42	-26.10	14.1	10.42	-26.10
10	22.68	20.84	-8.11	14.22	12.08	-15.05	14.22	11.62	-18.28	14.22	11.62	-18.28
9	23.58	20.84	-11.62	15.09	13	-13.85	15.09	12.78	-15.31	15.09	12.78	-15.31
8	24.05	20.84	-13.35	15.39	14.48	-5.91	15.39	14.88	-3.31	15.39	14.88	-3.31
7	26.86	20.84	-22.41	16.88	17.76	5.21	16.88	15.63	-7.41	16.88	15.63	-7.41
6	27.45	20.84	-24.08	17.44	20.84	19.50	17.44	19.2	10.09	17.44	19.18	9.98
5	34.55	25.04	-27.53	22.35	23.24	3.98	22.35	23.24	3.98	22.35	23.24	3.98
4	45.81	29.76	-35.04	28.5	29.76	4.42	28.5	29.01	1.79	28.5	29.01	1.79
3	54.08	41.68	-22.93	34.07	38.36	12.59	34.07	38.36	12.59	34.07	38.36	12.59
2	79.76	59.88	-24.92	50.36	58.02	15.21	50.36	58.02	15.21	50.36	58.02	15.21
1	154.98	116.04	-25.13	98.44	116.04	17.88	98.44	116.04	17.88	98.44	116.04	17.88

TABLE VI
COMPARISON OF SHIFTING TIME PER TEST PATTERN FOR hCADT02 WITH SEQUENTIAL TESTING

	$P_{ave} = 4000$			$P_{ave} = 8000$			$P_{ave} = 12000$			$P_{ave} = \infty$		
W_{ext}	T_r	T_{new}	$\Delta T(\%)$	T_r	T_{new}	$\Delta T(\%)$	T_r	T_{new}	$\Delta T(\%)$	T_r	T_{new}	$\Delta T(\%)$
32	57.6	48	-16.67	35.5	24	-32.39	32.05	13.8	-56.94	26.05	13.8	-47.02
31	57.6	48	-16.67	35.5	24	-32.39	32.05	13.96	-56.44	26.05	13.96	-46.41
30	57.76	48	-16.90	35.58	24	-32.55	32.09	18.18	-43.35	26.09	15	-42.51
29	71.4	48	-32.77	42.4	24	-43.40	35.5	19.2	-45.92	29.5	15.04	-49.02
28	71.4	48	-32.77	42.4	24	-43.40	35.5	24	-32.39	29.5	16	-45.76
27	71.4	48	-32.77	42.4	24	-43.40	35.5	24	-32.39	29.5	17.44	-40.88
26	71.4	48	-32.77	42.4	24	-43.40	35.5	24	-32.39	29.5	18	-38.98
25	71.48	48	-32.85	42.44	24	-43.45	35.54	24	-32.47	29.52	18	-39.02
24	83.4	48	-42.45	48.4	24	-50.41	41.5	24	-42.17	32.5	18.18	-44.06
23	83.4	48	-42.45	48.4	24	-50.41	41.5	24	-42.17	32.5	19.2	-40.92
22	83.48	48	-42.50	48.44	25.44	-47.48	41.54	24	-42.22	32.54	20.7	-36.39
21	89.8	48	-46.55	51.6	25.6	-50.39	44.7	24	-46.31	35.7	21	-41.18
20	89.8	48	-46.55	51.6	25.6	-50.39	44.7	24	-46.31	35.7	24	-32.77
19	89.8	48	-46.55	51.6	27.6	-46.51	44.7	24	-46.31	35.7	24	-32.77
18	89.8	48	-46.55	51.6	27.6	-46.51	44.7	25.44	-43.09	35.7	25.44	-28.74
17	89.8	48	-46.55	51.6	27.6	-46.51	44.7	25.6	-42.73	35.7	25.6	-28.29
16	101.8	48	-52.85	57.6	27.6	-52.08	50.7	27.6	-45.56	38.7	27.6	-28.68
15	102.12	48	-53.00	57.76	36.36	-37.05	50.78	34.5	-32.06	38.78	30	-22.64
14	115.6	48	-58.48	64.5	40	-37.98	54.15	36	-33.52	42.15	32	-24.08
13	115.6	48	-58.48	64.5	41.4	-35.81	54.15	36	-33.52	42.15	35.6	-15.54
12	127.6	48	-62.38	70.5	48	-31.91	60.15	40	-33.50	45.15	36	-20.27
11	127.76	50.88	-60.18	70.58	48	-31.99	60.23	41.4	-31.26	45.23	40	-11.56
10	134.64	51.2	-61.97	74.02	48	-35.15	63.55	48	-24.47	48.51	48	-1.05
9	159.8	55.2	-65.46	86.6	50.88	-41.25	72.8	50.88	-30.11	54.8	50.88	-7.15
8	171.89	55.2	-67.89	92.69	55.2	-40.45	78.89	55.2	-30.03	57.89	52.31	-9.64
7	207	80	-61.35	111.7	71.2	-36.26	94.45	64	-32.24	70.45	64	-9.16
6	219.79	96	-56.32	118.11	72.72	-38.43	100.67	72	-28.48	73.67	72	-2.27
5	255.62	96	-62.44	137.6	96	-30.23	116.67	96	-17.72	86.59	96	10.87
4	327.37	110.4	-66.28	174.97	110.4	-36.90	147.37	110.4	-25.09	108.37	104.61	-3.47
3	420.14	145.44	-65.38	222.8	144	-35.37	187.93	144	-23.38	136.93	144	5.16
2	616.16	240.64	-60.95	325.54	240.64	-26.08	273.23	240.64	-11.93	198.03	240.64	21.52
1	1228.63	481.28	-60.83	647.42	481.28	-25.66	542.81	481.28	-11.34	392.41	481.28	22.65

scan architecture when $P_{\text{ave}} = 4500$ (given in column 11 in Table III). However, after applying the method proposed in this paper, its testing time can be further reduced as shown in column 12 in Table III. Therefore, the proposed method is orthogonal to and it can be used in conjunction with scan chain segmentation to further improve the testing time under the given power constraints.

VI. Conclusion

Embedded cores with multiple clock domains are common practice nowadays. However, most published techniques for test wrapper design have been limited to single-frequency cores. This paper presented a 1500-compliant wrapper that prevents clock skew and reduces test power by allowing scan chains in different clock domains to shift test data at distinct frequencies. As a consequence, the proposed method improves upon a recent wrapper design method [6] for cores with multiple clock domains that requires a common shift frequency for the cores in the different clock domains. We have presented an ILP model that can be used to minimize the testing time for small problem instances, and which can be combined with LP-relaxation to obtain lower bounds on the testing time for large values of W_{ext}. We have also presented an efficient heuristic method that is applicable to large problem instances and compared to the recent wrapper design using a common shift clock, we obtain lower testing times, and the reduction is especially significant when scan chains are not well balanced between different clock domains.

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