CENG 4480
Lecture 10: Clock

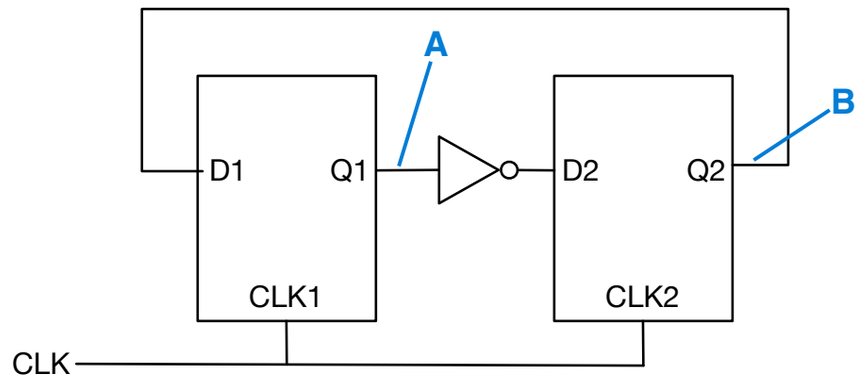
Bei Yu

Reference:

- Chapter 11 Clock Distribution
- **High speed digital design**
- by Johnson and Graham

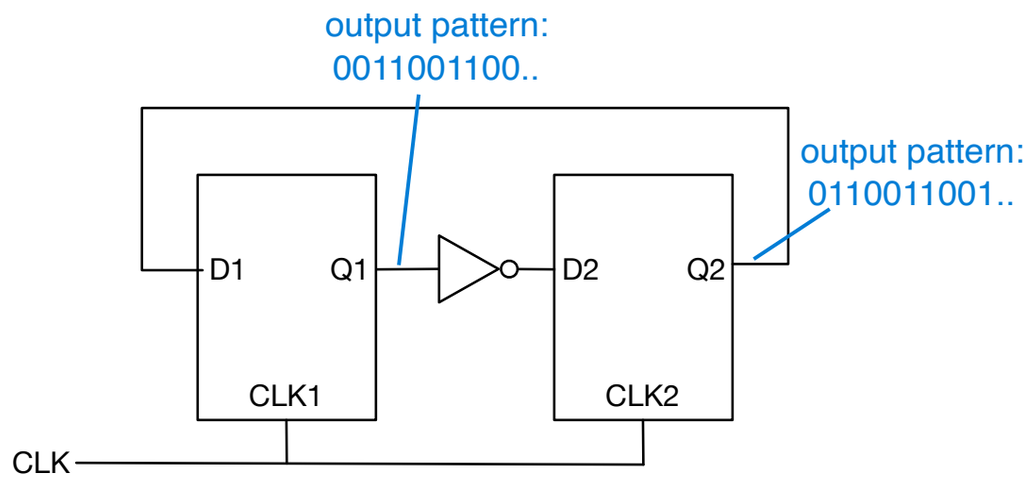
A 2-bit ring counter example

- 2-bit ring counter
- Initially A = B = 0; A = 0011001100
- What is B?



A 2-bit ring counter example

- The result is Okay when clock is slow
- But, when clock is TOO fast, get some problem



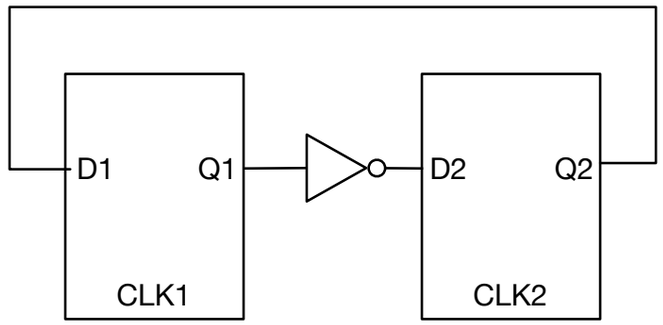
Arduino uno: 16 MHz

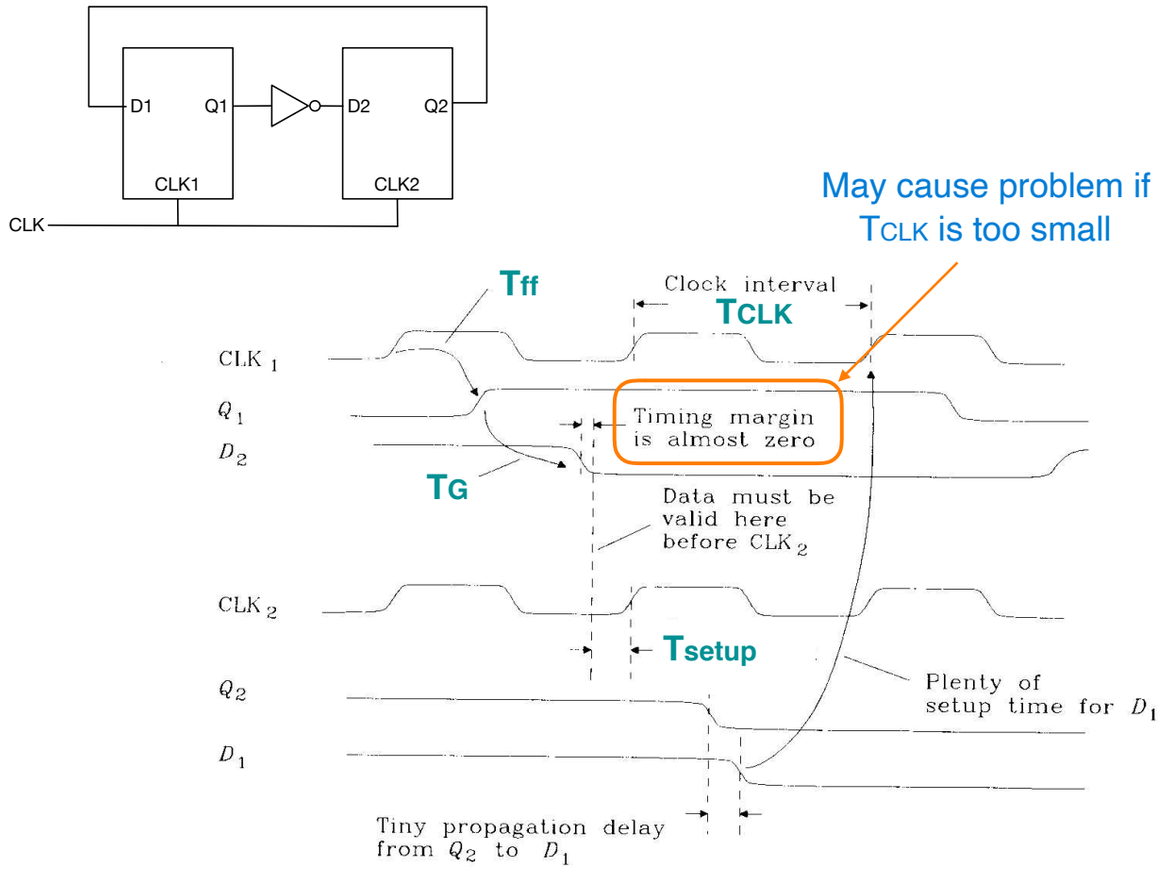
Setup Time and Time Margin

- Setup Time: The time that the input data must be stable before the clock transition of the system occurs
- Time Margin: measures the **slack**, or excess time, remaining in each clock cycle
  - Protects your circuit against signal cross-talk, miscalculation of logic delays, and later minor changes in the layout
  - Depends on both time delay of logic paths and clock interval

Notations in Clock Skew Calculation

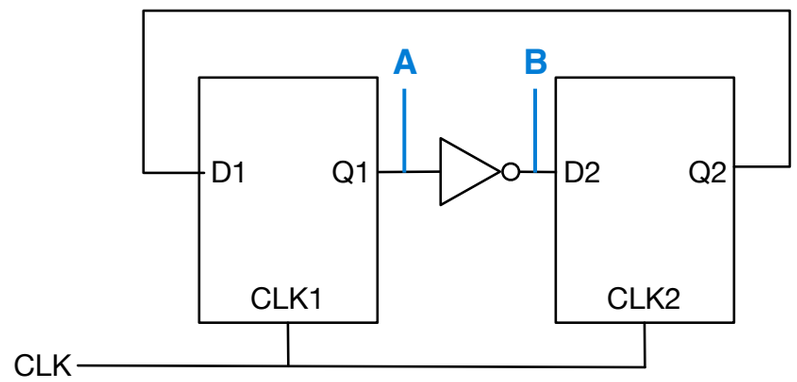
- **T_{ff}**: delay of flip-flop (FF)
- **T_G**: delay of gate G, including track delay
- **T_{setup}**: worst-case setup time required by FF2, data at D2 must arrive at least T_{setup} before CLK_2
- **T_{CLK}**: clock period; interval between clocks




D1
Q1
D2
Q2
CLK1
CLK2
CLK
May cause problem if
TCLK is too small
Tff
Clock interval
TCLK
CLK 1
Q 1
D 2
Timing margin
is almost zero
TG
Data must be
valid here
before CLK 2
CLK 2
Tsetup
Q 2
D 1
Plenty of
setup time for D 1
Tiny propagation delay
from Q 2 to D 1

EX. B2-1

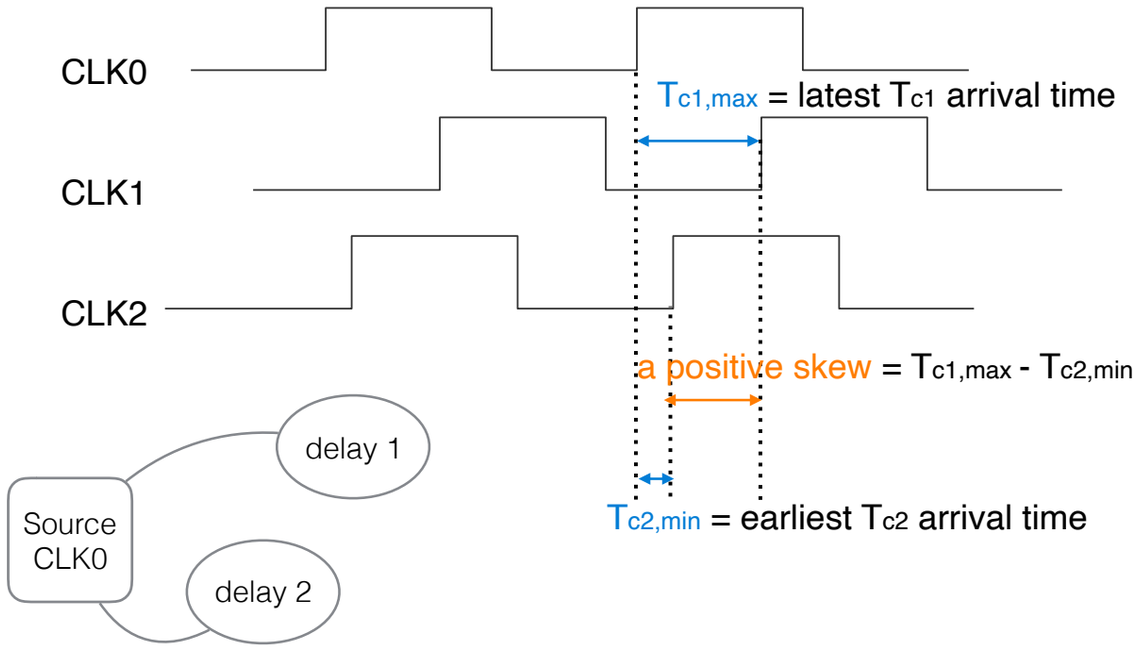
- CLK1 = CLK2 = 20MHz; T_{ff} = 8ns; T_{setup} = 5ns; T_G = 10ns.
- **Questions**:
  - Find time margin
  - How many delay G gates can you insert between A and B without creating error?



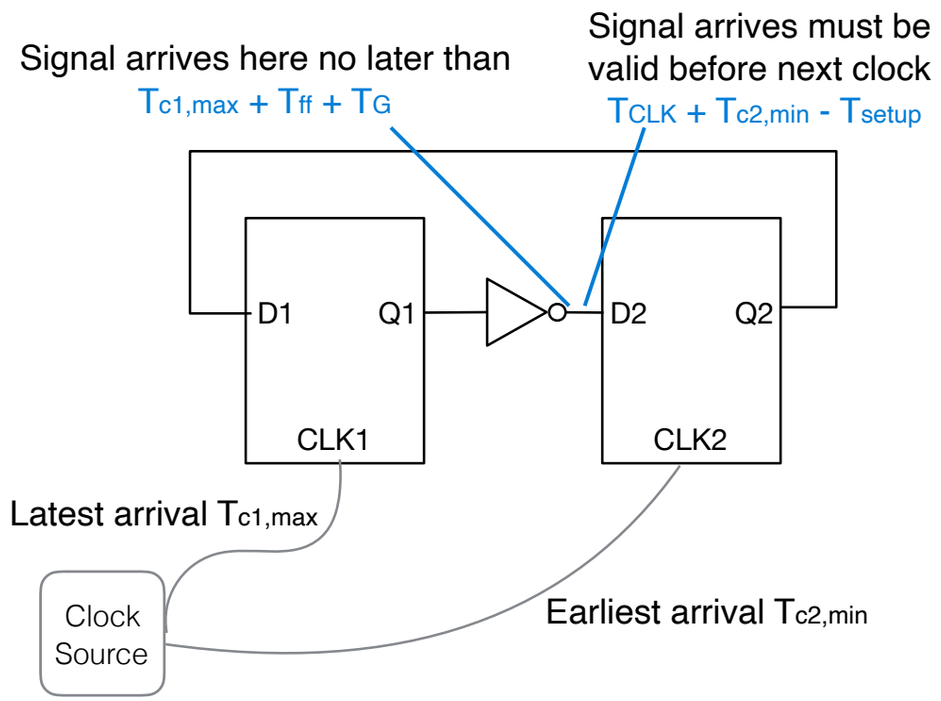
20MHz = 50 ns

Clock Skew

- The clock does NOT reach FF1, FF2 at the same time

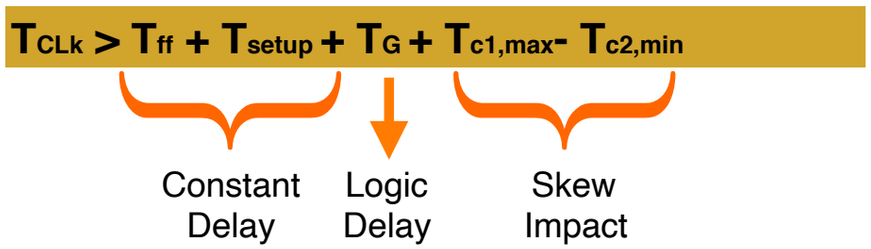


Why Care Clock Skew?



Why Care Clock Skew?

- $T_{delay} = T_{c1,max} + T_{ff} + T_G$
- $T_{clk'} = T_{CLK} + T_{c2,min} - T_{setup}$
- Since $T_{delay} < T_{clk'}$ =>



EX. B2-2

Question: Given

- T_{ff} = 7ns;
- T_G = 5ns;
- T_{setup} = 4ns;
- T_{CLK} = 40MHZ;

What's the biggest time skew allowed?

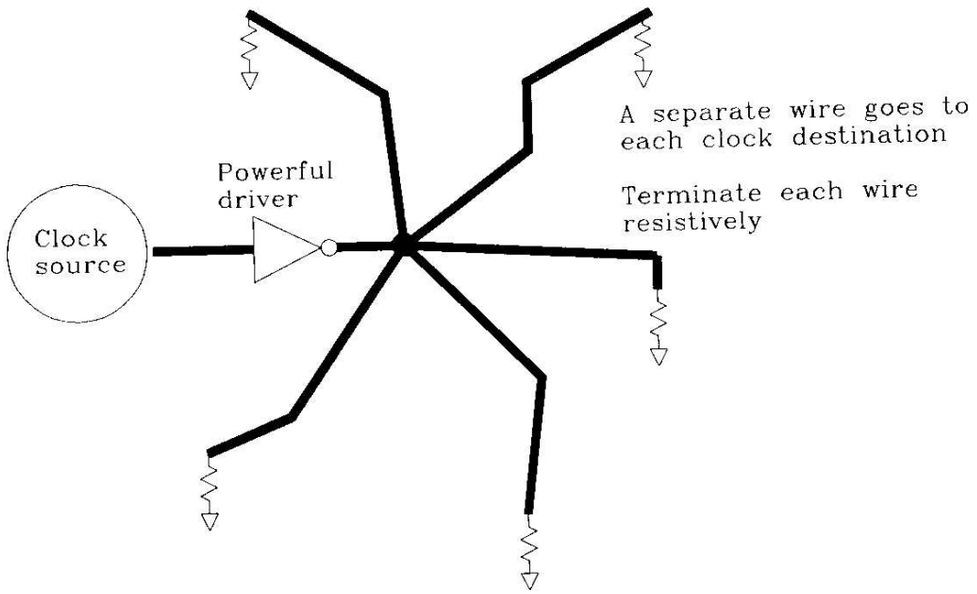
Answer:

40MHz = 4 x 10^7 cycles per second = 25 ns

Strategies to reduce clock skew

- Drive them from the same source & balance the delays
- Style 1: Spider-leg distribution network
  - use a power driver to drive N outputs.
  - Use load (R) termination to reduce reflection if the traces are long (distributed circuit). Total load =R/N.
  - Two or more driver outputs in parallel may be needed.
- Style 2: Clock distribution tree

Style 1: Spider-leg Clock



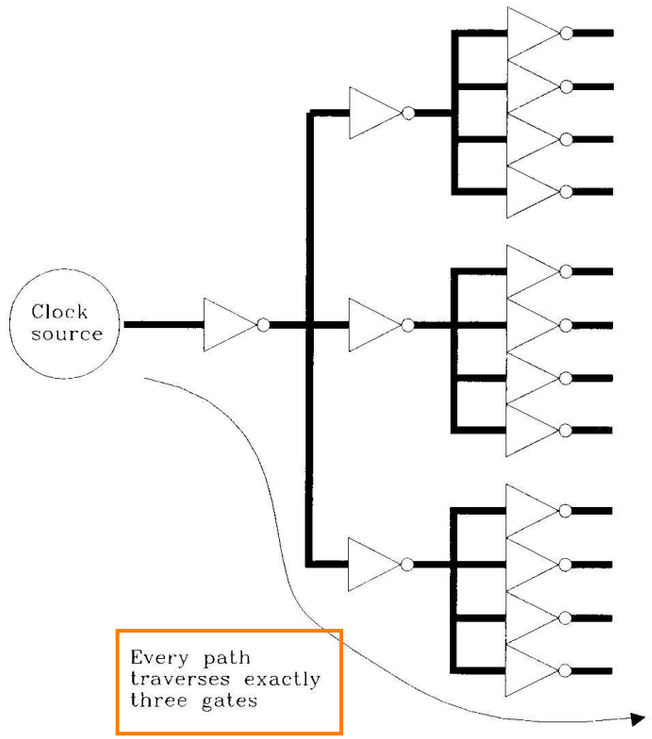
Distributes clocks from a single source to N remote destinations.

Reflections are damped by resistive terminations R at the end of each spider leg.

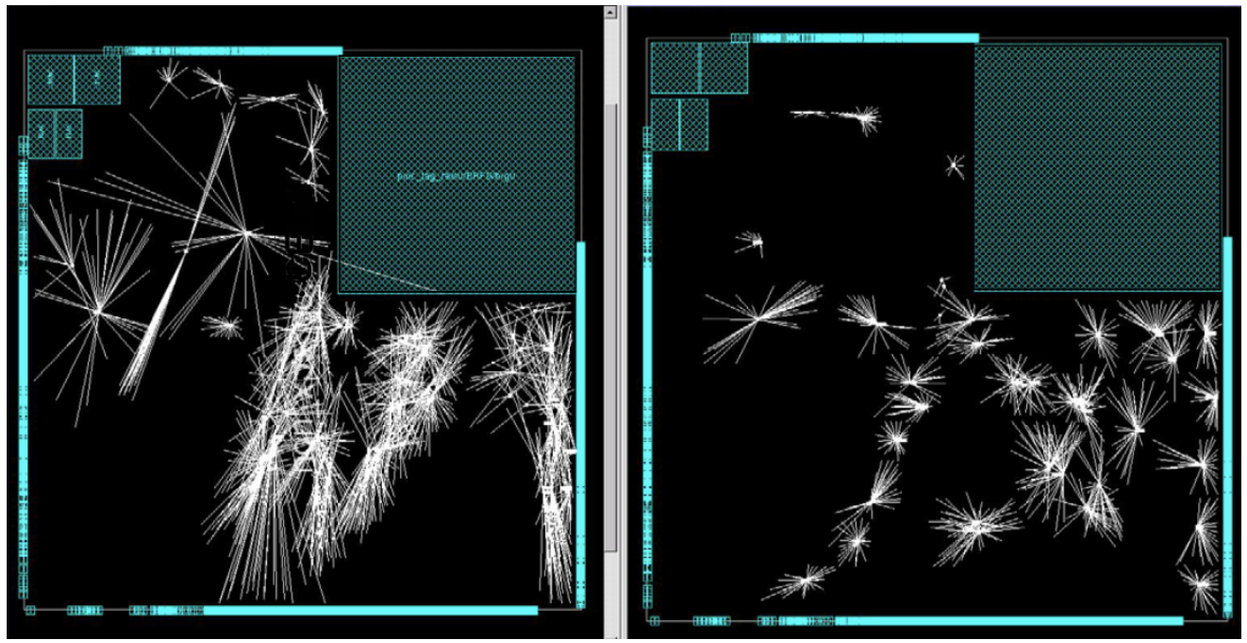
The drive circuit experiences a total load of R/N.

We need a more powerful clock driver.

Style 2: Clock Tree

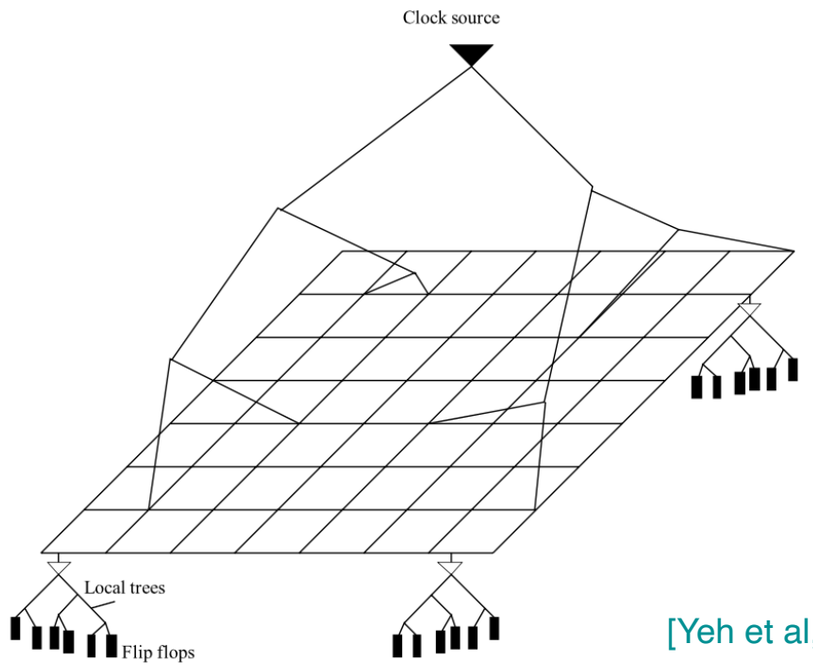


Modern Clock Design — 1



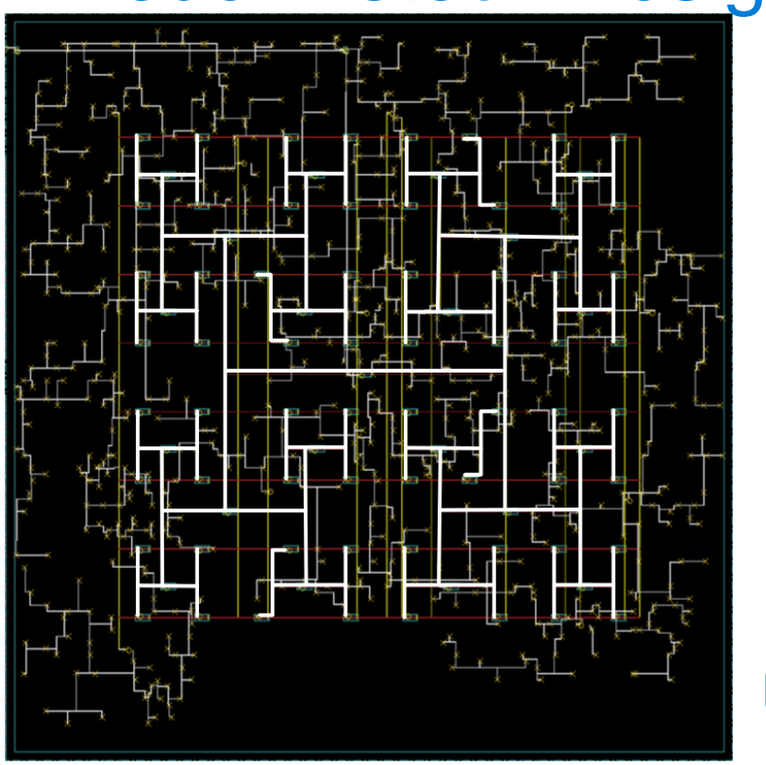
[Ho et al, ISPD'2009]

Modern Clock Design — 2



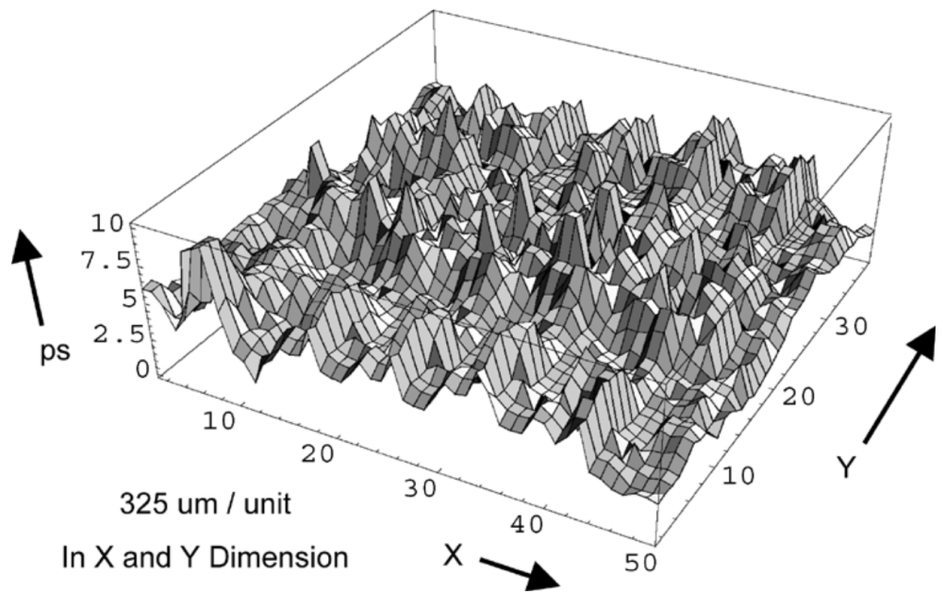
[Yeh et al, ISQED'2006]

Modern Clock Design — 3



[Seok et al, ISLPED'2010]

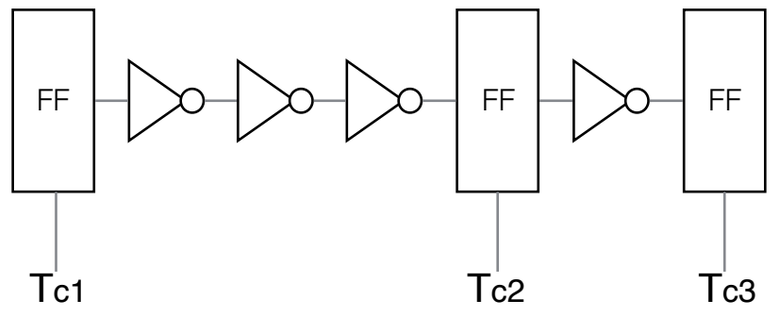
Clock Skew Distribution



[Pham et al, JSSC'2006]

EX. Skew Optimization

- Instead of Zero-Skew, take advantage of Skew.
- Question: Given T_G=6ns, T_{ff}=10ns, T_{setup}=2ns, what's the minimal T_{CLK}? Assume $T_{c3} = 0$.



Thank You