## CENG 3420 Quiz 1

## **Solutions**

Q1 Consider three different processors P1, P2, and P3 executing the same instruction set with the clock rates and CPIs given in the following table.

Processor	Clock Rate	CPI
P1	2 GHz	0.8
P2	3 GHz	1.2
P3	4 GHz	1.8

- 1. Which processor has the highest performance expressed in instructions per second?
- 2. If the processors each execute a program in 10 seconds, find the number of cycles and the number of instructions.

**A1** 1. 
$$IPS = \frac{\text{clock rate}}{CPI}$$
.

• 
$$IPS_1 = \frac{2 \times 10^9}{0.8} = 2.5 \times 10^9$$
;

• 
$$IPS_2 = \frac{3 \times 10^9}{1.2} = 2.5 \times 10^9$$
;

• 
$$IPS_3 = \frac{4 \times 10^9}{1.8} \approx 2.2 \times 10^9$$
.

Therefore, P1 and P2 both have the highest performance.

2. Number of cycles (*C*#) are calculated as follows:

• 
$$C\#_1 = 2 \times 10^9 \times 10 = 2 \times 10^{10}$$
;

• 
$$C#_2 = 3 \times 10^9 \times 10 = 3 \times 10^{10}$$
;

• 
$$C#_3 = 4 \times 10^9 \times 10 = 4 \times 10^{10}$$
;

3. Number of instructions (I#) are calculated as follows:

• 
$$I\#_1 = \frac{C\#_1}{0.8} = 2.5 \times 10^{10}$$
;

• 
$$I\#_2 = \frac{C\#_2}{1.2} = 2.5 \times 10^{10}$$
;

• 
$$I\#_3 = \frac{C\#_3}{1.8} \approx 2.2 \times 10^{10}$$
;

**Q2** Dividing 1001011 by 1001

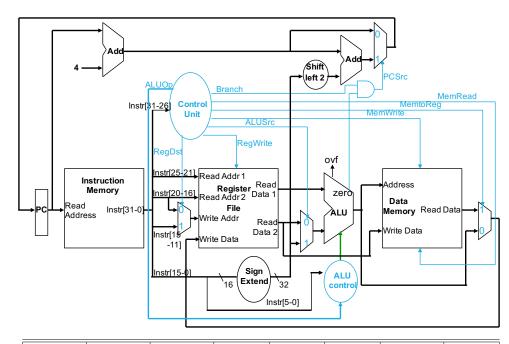
**A2** 1001011/1001 = 1000, and the remaindor is 0011. (011, 11) is also correct

**Q3** In a **Big Endian** machine, given the following code sequence and memory state:

add \$s2, \$zero, \$zero lb \$t0, 2(\$s2) sb \$t0, 5(\$s2)

Memory	
0x 0 0 0 0 0 0 0 0	24
0x 0 0 0 0 0 0 0 0	20
0x 0 0 0 0 0 0 0 0	16
0x 1 0 0 0 0 0 1 0	12
0x 0 1 0 0 0 4 0 2	8
0x F F F F F F F F	4
0x 0 0 9 0 1 2 A 0	0
Data	

- 1. What value is left in \$\pm 0?
- 2. What word is changed in Memory and to what?
- 3. What if the machine was **Little Endian**?
- **A3** 1.  $$t0 \leftarrow 0x00000012;$ 
  - 2. mem(5)  $\leftarrow$  0xFF12FFFF;
  - 3.  $$t0 \leftarrow 0x00000090$ , and mem (5)  $\leftarrow 0xFFFF90FF$ .
- **Q4** Given following datapath, provide the control signal for R-type instruction (in the following table). Branch & ALUOp signals have been in the table.



RegDst	ALUSrc	MemReg	RegWr	MemRd	MemWr	Branch	ALUOp
1	0	0	1	0	0	0	10