Test Pattern Selection for Potentially Harmful Open Defects in Power Distribution Networks

Yubin Zhang†, Lin Huang†, Feng Yuan†, and Qiang Xu†‡
†CUhk REliable computing laboratory (CURE)
Department of Computer Science & Engineering
The Chinese University of Hong Kong, Shatin, N.T., Hong Kong
‡CAS-CUHK Shenzhen Institute of Advanced Integration Technology
Email: {ybzhang,lhuang,fyuan,qxu}@cse.cuhk.edu.hk

ABSTRACT

Power distribution network (PDN) designs for today's high performance integrated circuits (ICs) typically occupy a significant share of metal resources in the circuit, and hence defects may be introduced on PDNs during the manufacturing process. Since we cannot afford to over-design the PDNs to tolerate all possible defects, it is necessary to conduct manufacturing test for them. In this paper, we propose novel methodologies to identify those potentially harmful open defects in PDNs and we show how to select a set of patterns that initially target transition faults to achieve high fault coverage for the PDN defects. Experimental results on benchmark circuits demonstrate the effectiveness of the proposed technique.

Keywords-power distribution network test; pattern sorting and selection; open defects; defect identification;

1. INTRODUCTION

For integrated circuits (ICs) fabricated with advanced semiconductor technology, the on-chip power distribution network (PDN) is responsible for providing accurate-enough power and ground voltages to every logic standard cell (SC) [20]. With the ever increasing circuit complexity, PDN designs for high-performance ICs have become increasingly challenging [7, 10] and they typically occupy a considerable part of metal resources in the circuit, e.g., 28% for a recent microprocessor [1].

Because of the above, it is very likely that defects are introduced on PDN during the manufacturing process [9, 17]. The total number of possible PDN defect locations is enormous and it is impossible to generate test for every one of them. Fortunately, typical PDN is essentially a defect-tolerant structure and a large number of PDN defects are in fact harmless, especially when the PDN is over-designed. However, it is extremely costly, if not impossible, to strengthen the PDN tolerating all possible defects, since such PDN designs would waste lots of crucial routing resources that can be used to improve the circuit performance.

Today, for those harmful PDN defects that cannot be tolerated, designers mainly rely on test patterns for stuck-at faults and delay faults to identify them implicitly. While the above implicit test strategy works quite well for relatively simple designs previously, with technology advances, PDN defects may cause substantial timing errors for high-performance ICs, which cannot be detected by regular delay tests. This is because: (i). the power supply noise margin of IC devices gets smaller and smaller with decreasing supply voltage in each new technology generation [4, 5], and circuit performance suffer to more extent from the power supply degradation. For example, it was shown that a 1% change for the supply voltage can result in nearly 4% change in circuit delay with 90nm technology [19]; (ii). the worst-case power supply caused by PDN defects occurs when the local switching activities surrounding the defective position are the maximum, which leads to severe power droop [2, 3, 18]; On the other hand, conventional test patterns that target for delay faults try to sensitize the logic paths so that the targeted delay error effects can be observed [8, 16], which may not activate intensive transitions near the PDN defect locations.

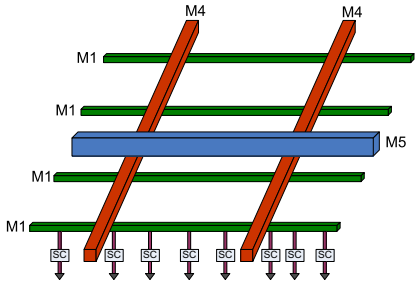


Figure 1: An example power distribution network.

It is therefore essential to identify those potentially harmful defects on the PDN and apply test patterns to detect them, ensuring the quality of the shipped products. Due to the huge number of possible PDN defect locations, this is an interesting and challenging problem. In this work, we first present novel techniques to efficiently extract a small set of vulnerable PDN locations, which contains all the potentially harmful defects. Secondly, we propose to select a set of 1-detect transition fault patterns out of the N-detect patterns [11] so that we are able to achieve high PDN defect coverage without increasing the test pattern count.

The remainder of this paper is organized as follows. Section 2 presents the preliminaries and the motivation of this work. The proposed potentially harmful defect identification methodology is shown in Section 3. Section 4 then presents our test pattern selection algorithm for PDN defect coverage improvement, under the constraint that all the testable transition faults are covered. Experimental results are presented in Section 5. Finally, Section 6 concludes this paper.

2. PRELIMINARIES AND MOTIVATION

2.1 PDN Structure and Modeling

Power distribution network is typically designed with a hierarchical structure, which traverses multiple metal layers in the circuit. Fig. 1 depicts a typical power network structure, which involves three metal layers (M1, M4, and M5 from bottom up). The wires on different metal layers are linked together through vias, and they are eventually connected to the power pads at the uppermost layer. The devices are arranged below M1 layer in rows, and obtain power supply from power wires on M1 layer. It can be easily observed that, PDN with such infrastructure is to a great extent defect-tolerant since the device can acquire power supply through multiple paths from the power pad. The ground network of the PDN, which is the counterpart of the power

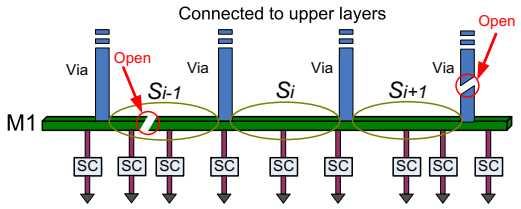


Figure 2: Segmented structure for PDN tracks on M1 layer and possible open defects.

network, is with similar structure and therefore is not shown in Fig. 1. Here in this paper, for clarity only the analysis for power network will be presented, while ground network is not mentioned because of the similarity unless it is with necessary to show the difference.

As can be observed from Fig. 1, the PDN structure on M1 metal layer typically consists of a group of parallel tracks while each track can be viewed as a series of wire segments, wherein a segment refers to a part of PDN wire on M1 between two vias, called *M1 segment* hereafter. An example of such M1 segments is shown in Fig. 2, which are marked as S_{i-1}, S_i and S_{i+1}. The open defects may occur on a via or a wire segment and an example open defect is demonstrated on Fig. 2. With the existence of PDN open defects, those SCs that normally draw current from the nearby wire/via would be forced to get power supply through longer paths. This can change the power supply topology and may induce insufficient supply voltage for certain SCs.

To model the PDN for analysis, let $\mathbf{G} = \{G_{i,j}\}$ be the conductance matrix of the PDN, namely *PDN matrix*, wherein $G_{i,j}$ represents the conductance between node i and j on PDN. In addition, $\mathbf{V} = \{v_j\}$ and $\mathbf{I} = \{i_j\}$ represent the voltage vector and the current vector of all the nodes, respectively. The analytical model for the PDN can then be expressed as $\mathbf{GV} = \mathbf{I}$. Here, $\mathbf{G}$ is extracted from layout information, and $\mathbf{I}$ corresponds to switching activity. The power supply voltage distribution on PDN can then be achieved by solving these linear equations [20], called PDN simulation in this paper.

2.2 Prior Work and Motivation

There are only limited works on PDN testing in the literature. Sato *et al.* [14] proposed a so-called box-scan method to identify weak positions in power distribution networks. Their method, however, is not applicable for industrial designs due to the high computational complexity. Recently, Ma *et al.* [9] proposed an automatic test pattern generation (ATPG) method for open defects on PDN. To reduce the problem complexity, this work proposes to divide the power distribution network into a number of regions and tries to activate as many switching activities in a region as possible for test generation. This strategy can be very effective for testing defects on high metal layers as they affect a relatively larger region at the circuit level. For defects on low metal layers (especially M1), however, their impacts are localized and activating switching activities for a sizable region may not be able to identify the error. As there are significantly more PDN defects on the denser low metal layers than that on higher ones, it is essential to develop new test methodologies for such defects, which motivates this work. In particular, we focus on open defects on the lowest PDN metal layer (say, M1) and vias that connect it to its neighboring PDN metal layer (say, M2) in this work, which usually covers more than 95% of the total possible PDN defects.

As discussed earlier, a great share of PDN defects are harmless for the design due to the defect-tolerance nature of PDN structure. On the other hand, because of the huge number of possible PDN defects, it is very difficult, if not impossible, to evaluate their effects by simulating them one by one. As a result, it is essential to identify those potentially harmful PDN defects in an effective and efficient manner. Then, to detect these harmful defects, we can either generate dedicated test patterns for them or select a set of delay test patterns to cover them implicitly. In this work, we take the latter approach and try to select a set of 1-detect transition fault patterns out of N-detect patterns that are able to achieve high PDN defect coverage.

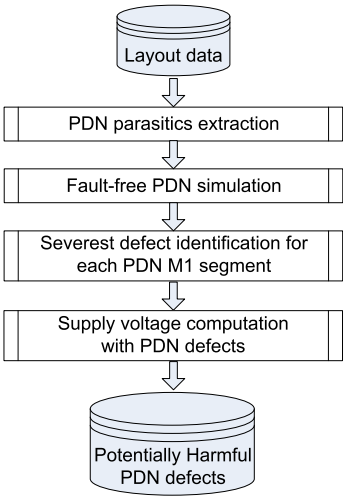


Figure 3: Flowchart of the proposed method for identifying potentially harmful PDN defects.

It should be highlighted that simply increasing the switching activities of the test patterns (e.g., by X-filling), although effective for the detect of PDN defects, is not a good solution. This is because: test patterns with prohibitively-large switching activities can result in serious over-testing problem [6, 15], since it increases the power supply noise of the circuit to an extent that cannot occur in functional mode and may reject some good chips that would work in application, thus leading to yield loss due to test overkills.

3. POTENTIALLY HARMFUL PDN DEFECTS IDENTIFICATION

In today's large ICs, there are millions of wire segments in the PDN and hence the number of possible open defects is enormous. It is very difficult, if not impossible, to evaluate the impact of all these defects by PDN simulation because of the extremely high time complexity. Based on the observation that most of these defects can be tolerated by the PDN infrastructure itself, we propose an efficient and effective approach to identify those PDN defects that *might* result in errors, which are referred to as *potentially harmful defects* in this paper.

3.1 Overall Flow

The main concern for the harmful PDN defect identification process is its time complexity. To handle this problem, we should perform the time-consuming PDN simulation process as few times as possible. The flowchart of the proposed harmful defect identification method is shown in Fig. 3 while the details are shown as follows.

PDN parasitics extraction: In this step, the parasitic information of the whole PDN is extracted from the circuit layout files. The extracted parasitic information is then transformed to feed the linear equation solver for PDN simulation. With N nodes in the PDN, a $N \times N$ matrix $\mathbf{G}$ need to be built. In addition, the mapping between the gates at logic level and the PDN nodes extracted from the layout information should also be constructed to build the current vector $\mathbf{I}$. The PDN analysis expressed as $\mathbf{GV} = \mathbf{I}$ can then be solved to produce the supply voltage distribution result $\mathbf{V}$.

Defect-free PDN simulation: To analyze the PDN system, we build a PDN simulator based on a linear equation solver [12, 13] to obtain the voltage of every node according to the relationship $\mathbf{GV} = \mathbf{I}$. The defect-free PDN can then be analyzed by the PDN simulator while the result will be further used in the following steps.

Severest defect identification for each PDN M1 segment: As the currents go through vias to M1 tracks of PDN and then to SCs, the severest open defect within each M1 segment, which usually contains tens of SCs and corresponding wires, must be on the wires next to the vias that are denoted as edge wires, since power supply to the SCs must be through the edge wires. The open defects on the edge wires

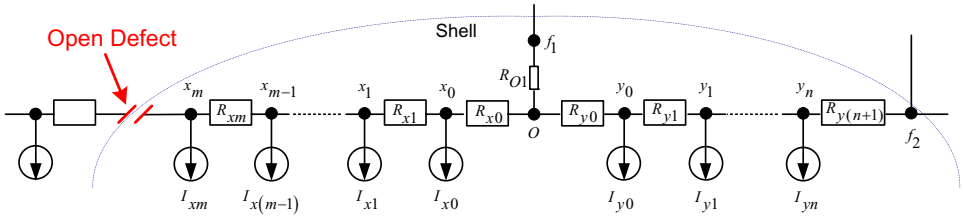


Figure 4: Distributed circuit model for the computation of PDN open defects induced power supply drop.

are correspondingly denoted as *edge defects* while the defects on the internal wires of M1 segments are denoted as *internal defects*. The two edge defects in each M1 segment will be evaluated by PDN simulation and the worse one will be the severest defect in this segment. If the worst open defect in an M1 segment cannot induce any function error, all the defects within this segment will not be considered as harmful defects any more since they are in fact tolerable defects. Such technique can greatly reduce the time complexity for identifying harmful defects, or excluding tolerable defects, since the defect tolerance characteristic and the specific power supply structure of PDN have been taken into account.

The PDN simulation times can be further reduced by simultaneous injection of multiple independent PDN defects into the circuit at one time for simulation, instead of injecting and simulating them one by one. Here, independence indicates the property that the effective regions of any two defects in this set do not overlap with each other while the effective region of a defect includes all the PDN nodes that may be influenced by such defect. As the effect of a defect on M1 layer is typically localized in a small region, high compaction ratio in defect simulations can be achieved because each defect is independent with most of other defects except its neighboring ones.

Besides identifying the severest defect in each M1 segment, the accurate voltage result from PDN simulation will be further used to calibrate the computation of the internal defects, which is detailed in the following.

Supply voltage computation with PDN defects: Recall that we cannot afford to evaluate all the possible open defects by PDN simulation and we need to pick out the most destructive ones in an efficient manner. Instead of running the time-consuming PDN simulation to obtain the supply voltage disturbance induced by PDN defects, we propose a fast computation method for the internal defects, which requires much less computational time. The details of the proposed computation algorithm is shown in section 3.2.

Finally, through either simulation or computation, the power supply voltage distribution induced by each PDN defect can be obtained, with which the defects that can result in severe supply voltage droop and function error are identified as potentially harmful PDN defects.

3.2 Computation of Voltage Drop Induced by PDN Defects

A fast yet accurate power supply distribution computation method is proposed in this section, which is composed of two steps: calculation and calibration. Calculation step aims to quickly obtain the voltage distribution while the calibration step adjusts the calculation results segment by segment for higher accuracy. By means of the proposed computation method, only the two edge defects in each segment need to be simulated while the effects of all the internal defects can be accurately computed. As the average quantity of SCs in each segment is typically around one hundred, this strategy can significantly cut down the time consumption.

The effective region of PDN defects on M1 layer is localized in a small domain, which indicates that, compared with that of the defect-free situation, only a small part of the PDN nodes will have voltage variation after the injection of such a defect. With a shell surrounding the whole effective region, we can then perform voltage calculation only on the nodes inside the shell while all other nodes are left alone with defect-free voltage value, which can greatly reduce the number of elements involved into the calculation.

We model SCs as current sources, and the wires between two PDN nodes as resistors. The distributed circuit model is constructed accordingly for supply voltage drop calculation, and an example is shown in Fig. 4. Setting V_{f1} and V_{f2} at the same values as that in defect-free situation, the shell for localized calculation is actually set as the node set including node f_1, f_2 and x_m in this example. The voltage calculation for all the SCs in the two segments (denoted as segment x and y, respectively) can then be localized in the region surrounded by these three nodes.

We denote by I_L and I_R the currents flowing out of node O to the left and right directions, respectively. Since all the standard cells within segment x are fed with current from node O, we have $I_L = \sum_{i=1}^{m} I_{xi}$. The SCs within segment y, on the other hand, are fed with currents from two vias while the current from the right via is given by $I_R = \frac{V_{f2}-V_{yn}}{R_{y(n+1)}}$. As the total current drawn by the SCs in segment y is $\sum_{j=1}^{n} I_{yj}$, the current drawn from the right side of node O is therefore $I_R = \sum_{j=1}^{n} I_{yj} - \frac{V_{f2}-V_{yn}}{R_{y(n+1)}}$. With these notations, we first build relation considering the current of node O by the following equation.

$$\frac{V_{f1}-V_O}{R_{O1}} = I_L + I_R = \sum_{i=1}^{m} I_{xi} + (\sum_{j=1}^{n} I_{yj} - \frac{V_{f2}-V_{yn}}{R_{y(n+1)}}) \quad (1)$$

After some algebra, we express the voltage of node O as

$$V_O = V_{f1} - R_{O1}(\sum_{i=1}^{m} I_{xi} + \sum_{j=1}^{n} I_{yj} - \frac{V_{f2}-V_{yn}}{R_{y(n+1)}}) \quad (2)$$

With V_O, we thereafter calculate the voltage for any node within these two segments. For example, the voltage of the k^{th} node in segment x, V_{xk}, can then be expressed as

$$V_{xk} = V_O - \sum_{i=0}^{k} (R_{xi} \sum_{j=i}^{m} I_{xj}) \quad (3)$$

Fig. 5 depicts the error between the calculated and simulated values of the minimum voltage caused all the defects in one segment. We observe that the errors follow approximately segmented linear distribution. We therefore further calibrate the results obtained by the fast calculation method as follows.

(I) Simulate the two edge defects in each segment;

(II) Calculate the supply voltage drop induced by all the defects through the localized calculation method proposed in the above;

(III) Calculate the errors between the simulated and the calculated voltage values for the two edge defect;

(IV) Calculate the errors for all the internal defects with the error value of the two edge defects and the segmented linear distribution, segment by segment;

(V) Calibrate the initial calculation results with the errors obtained in (IV) for each internal defect.

Apparently, the proposed voltage computation method, composed of fast calculation and accurate calibration, can be finished in neglectful time compared with defect simulation because such computation is localized and can be completed straightforward while the defect simulation is performed globally with multiple iterations.

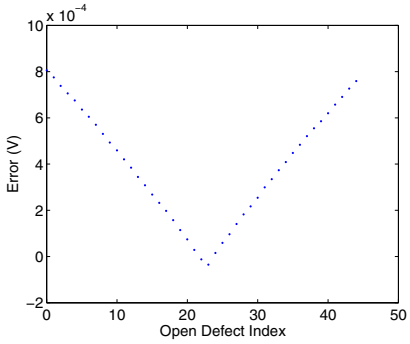


Figure 5: Errors between the simulated and computed values.

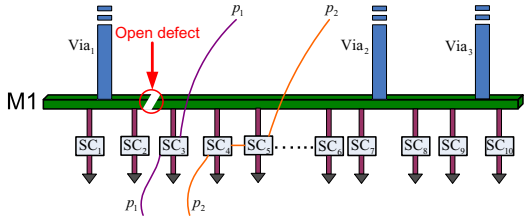


Figure 6: PDN defect detection via exercising transition faults in the circuit.

4. TEST PATTERN SORTING AND SELECTION METHODOLOGY

To detect potential harmful PDN open defects, we need to visualize these defects with test patterns so that the chips with such defects can be screened out. In this section, we propose to select test patterns for PDN defects from the transition fault test patterns while the generation of dedicated PDN test patterns is out of the scope of this paper and will be addressed in the future.

4.1 PDN Defect Detection

The existence of PDN open defects change the topology of power supply so that certain SCs cannot be fed with adequate supply voltage. Therefore, in order to detect PDN defects, it is essential for the test patterns to activate dense switching activity in the corresponding effective region to burden the power supply during testing. In addition, since we expect delay errors at the observing points if harmful PDN defects occur, test patterns should also be able to activate paths through the SCs with extra delay due to insufficient power supply induced by PDN defects. The combination of power activation and path activation at the same time can then demonstrate the existence of harmful PDN defects.

An example of PDN defect detection is illustrated in Fig. 6. Because of the open defect, some standard cells (e.g., SC_3 in Fig. 6) have to draw currents from the faraway via_2 instead of from the nearby via_1 as in the defect-free situation, which results in more power supply drop on these SCs compared with the defect-free situation. To detect the defect, we need to activate heavy current drawn from the SCs at the right side of the PDN defect with test patterns. In addition, the paths through the standard cells inside the effective region with severe power supply (i.e., p_1 and p_2) should be activated to propagate the long delay of those affected SCs out to primary outputs (POs) or pseudo-primary outputs (PPOs).

4.2 Overall Flow of Pattern Sorting and Selection Procedure

The flowchart of the proposed test pattern sorting and selection methodology is shown in Fig. 7, and the details are explained as follows.

Transition fault simulation: In this step we run transition fault simulation to identify the transition faults that can be detected by each test pattern.

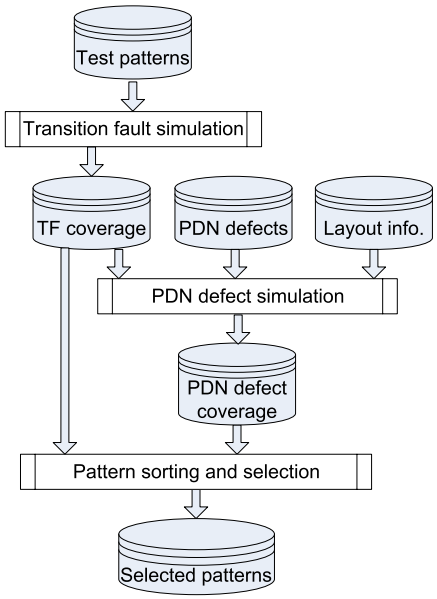


Figure 7: Flowchart of the pattern sorting and selection methodology.

PDN defect simulation: The goal of PDN defect simulation is to identify the PDN defects that can be detected by each pattern while three main tasks are needed to be performed on all the patterns one by one to achieve such purpose.

(I) Logic simulation: With a given pattern stating the logic values of Primary Inputs (PIs) and scan cells, the values of all the logic gates can be obtained by logic simulation. The transition information of all the SCs inside the circuit can then be collected. Thereafter, the exact current activated by each pattern can be known and such information can then be used to build the current vector **I**. As a result, each test pattern is with a corresponding vector **I**.

(II) Power supply distribution computation: In order to identify the PDN defects covered by a pattern, we need to compute the power supply distribution induced by each defect under the application of such pattern. That is, computation for every combination of one pattern and one defect is needed while the straightforward method of circuit simulating for each of such combinations will cost prohibitive time. The proposed voltage calculation/calibration method and the simulation of multiple independent defects, shown in section 3, will also be applied here, which greatly reduces the run time. That is, defect-free PDN simulation is performed for each pattern at first; Only the edge defects in the segments with potentially harmful PDN defects will be simulated with the injection of multiple independent defects in each time; For other defects, the corresponding induced supply voltage distribution will be obtained by calculation and calibration instead of PDN simulation.

(III) PDN defect identification: With the voltage distribution for each pattern with the existence of every defect, the PDN defects that can be detected by each pattern can then be identified. If a test pattern p can detect the transition fault of a standard cell whose power supply is lower than a pre-defined threshold in the existence of PDN defect d, it is then collected that pattern p can detect defect d.

Pattern sorting and selection: Given a set of n-detect transition fault patterns, our objective is select a subset to cover all the transition faults and detect as many PDN defects as possible. We propose a greedy heuristic to tackle this problem, as detailed in Section 4.3.

4.3 Pattern Sorting and Selection Algorithm

In this section, we propose to sort and select a list of test patterns from a group of candidates. We first find out the transition faults and PDN defects that can be detected by each pattern. Thereafter, the transition fault coverage, R_{tf}, and the PDN defect coverage, R_{pdn}, of each pattern can be computed. These data are summarized into a

pattern	TF detected	R_{tf}	PDN defects detected	R_{pdn}
p_0	tf_0, tf_5, tf_{16}	6%	d_1, d_7, d_9	15%
p_1	tf_5, tf_9	4%	d_3, d_{12}	10%
...	...	...	...	...
p_n	$tf_1, tf_3, tf_{11}, tf_{19}$	8%	$d_6, d_{14}, d18$	15%

Table 1: Transition faults and PDN defects coverage table.

Fault and Defect Coverage Table (FDCT) while an example is shown in Table 1.

To evaluate the effectiveness of test patterns, we need to consider both transition fault and PDN defect coverage. A metric is therefore proposed, denoted as weighted coverage R_t.

$$R_t = a \times R_{tf} + b \times R_{pdn} \tag{4}$$

where a and b are weight parameters that reflect the relative importance of different kinds of fault coverage. Instead of using fixed a and b during the pattern selection procedure, we propose to adjust them at each step to achieve better pattern selection effect in the following manner.

$$\frac{a}{b} = \frac{1 - C_{tf}}{1 - C_{pdn}} \tag{5}$$

C_{tf} and C_{pdn} are the fractions of transition fault covered by the presently selected pattern set and that of PDN defect respectively. The parameters of a and b dynamically changing in such a way can reflect the updated coverage information, which can therefore achieve balanced coverage between transition fault and PDN defect. At the same time, such technique enables the pattern that can improve the total coverage most with high priority to be selected. As long as $1 - C_{pdn} \neq 0$, we always set b to 1, and compute a by Eq. 5. Specially we set $a = 1$ and $b = 0$ when $1 - C_{pdn} = 0$. For example, suppose $C_{tf} = 30\%$ and $C_{pdn} = 50\%$, which means that there are 70% of transition faults and 50% of PDN defects uncovered by the presently selected pattern set. We have $a = 1.4$, the patterns with high transition fault coverage are more preferable to be selected so that the transition fault coverage can be improved faster than that of the PDN defect.

The procedure to sort the n-detect patterns, which can test each of the faults by n times, and select a subset of them to achieve high PDN defect coverage is shown in Fig. 8. This algorithm takes the fault and defect coverage table T of the n-detect patterns as input and produces a sorted subset of the patterns, P_L. At the beginning, P_L is initialized to be empty while the number of left patterns, n_{lp}, is initialized as the total number of available test patterns, N_p; the uncovered transition fault list, L_{tf}, initially contains all the transition faults F and the uncovered PDN defect list, L_{pdn}, contains all the PDN defects D (Line 1). One pattern will be selected into P_L during each iteration (Lines 2-14). At the beginning of each iteration, parameters a and b are computed according to Eq. 5 (Line 3). All the patterns are evaluated with respect to transition fault and PDN defect coverage (Lines 6-7) and the pattern with maximum R_t is selected into P_L (Line 9). After the selection of one pattern, all the related information should be updated (Lines 11-14): the selected pattern, p_{sel}, is appended to the selected pattern list (Line 11); all the transition faults that can be detected by the selected pattern, $T_{tf}[sel]$, are removed (denoted by the symbol $\setminus$) from the uncovered transition fault list (Line 12) and all PDN defects that are covered by the selected pattern, $T_{pdn}[sel]$, are removed from the uncovered PDN defect list (Line 13); the table T should also be updated by removing the row corresponding to the selected pattern (Line 14). The procedure will terminate if the maximum weighted coverage $R_{max} = max(R_t)$ is no greater than zero or there is no unselected pattern left. Finally, the selected and sorted test patterns are returned (Line 15).

5. EXPERIMENTAL RESULTS

To demonstrate the effectiveness of the proposed methodology, we have applied it on ISCAS'89 benchmark circuit s38417, which has 134 I/O ports and 23815 DFF/gates. Firstly, we generate the layout of

Pattern Selection Algorithm

INPUT: Table T
OUTPUT: Selected Patterns P_L

1. initialize $P_L \leftarrow \emptyset$; $n_{lp} \leftarrow N_p$; $L_{tf} \leftarrow F$; $L_{pdn} \leftarrow D$;
2. **while** $n_{lp} > 0$
3. $\quad \frac{a}{b} \leftarrow \frac{|L_{tf}|/|F|}{|L_{pdn}|/|D|}$;
4. $\quad R_{max} \leftarrow 0$; $sel \leftarrow -1$
5. $\quad$ **for** $i = 0$ to $|T| - 1$
6. $\quad\quad$ compute $R_{tf}[i]$ and $R_{pdn}[i]$;
7. $\quad\quad R_t[i] \leftarrow aR_{tf}[i] + bR_{pdn}[i]$;
8. $\quad\quad$ **if** $R_t[i] > R_{max}$
9. $\quad\quad\quad R_{max} = R_t[i]$; $sel = i$;
10. $\quad$ **if**($R_{max} \leq 0$) break;
11. $\quad P_L = P_L \cup \{p_{sel}\}$;
12. $\quad L_{tf} = L_{tf} \setminus T_{tf}[sel]$;
13. $\quad L_{pdn} = L_{pdn} \setminus T_{pdn}[sel]$;
14. $\quad T = T \setminus T[sel]$;
15. **return** P_L;

Figure 8: Procedure of the proposed pattern sorting and selection algorithm.

this circuit using a commercial tool and the corresponding parasitic information is then extracted from such layout. The power supply voltage V_{dd} is set at 1.2V corresponding to the layout library.

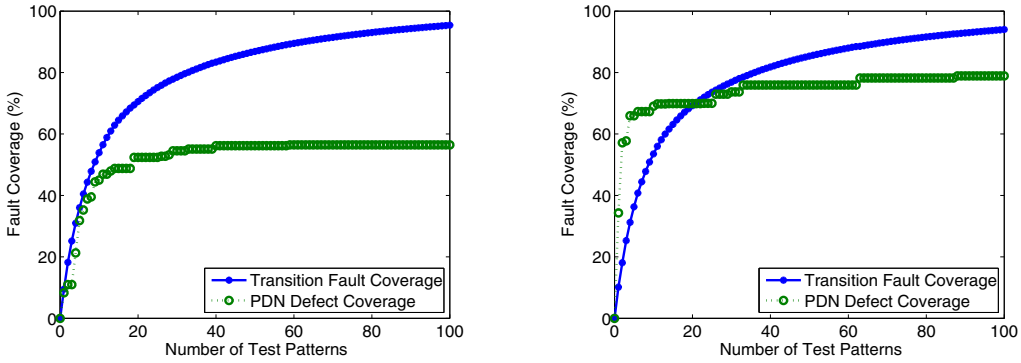
Given no PDN open defects, all SCs can get power supply voltage higher than 94% V_{dd} with transition probability of 37.5%, according to the simulation results. The threshold voltage V_{th} for transition fault is at 90% V_{dd}, implying that there will be a slow-to-rise transition fault happening to the SCs that intend to make a rising transition but are provided with power supply voltage lower than V_{th}. In addition, we generate a 5-detect transition fault test pattern set by a commercial tool, and we intend to select a 1-detect pattern set out of it and compare the selected set against the 1-detect set directly generated from the same tool.

In the potentially harmful defects identification process, we set the transition probability as 37.5% to compute the current vector **I**. By using the proposed defect simulation and computation method presented in section 3, 840 open defects are identified as potentially harmful, which is about 3.5% of the total number of possible defects inside the whole PDN (around 25K). The existence of any of these defects may potentially induce insufficient power supply on one or more SCs (i.e., lower than the threshold voltage V_{th}).

Then, we evaluate the PDN defect coverage by the original 1-detect test pattern set, which is composed of 416 patterns and have a transition fault coverage of 97.79%. The PDN defect coverage by up to 100 patterns are depicted in Fig. 9(a). With this set, totally 57.02% of the potentially harmful PDN defects can be detected.

Next, we select a set of 1-detect test patterns from the 5-detect patterns (including 1999 test patterns) to cover all the testable transition faults and at the same time we intend to cover as many PDN defects as possible, using the proposed strategy described in section 4. Fig. 9(b) shows the transition fault and PDN defect coverage variation with respect to the selected pattern count. With the proposed methodology, 366 patterns are selected to cover all the testable transition faults, which is even smaller than the original 1-detect test set. More importantly, the total PDN defect coverage is increased to 79.40%, which is 1.39 times of that of the original 1-detect pattern set.

The remaining 20.6% (173 out of 840) of the potentially harmful defects cannot be detected by all the patterns. We attribute them to: (i). some of the identified potentially harmful PDN defects can indeed be tolerated by the PDN structure; (ii). some PDN defects need more intensive switching activities to induce severer power supply droop so that they can be detectable, but the transition patterns are generated without such consideration and hence even the 5-detect test set may not be able to visualize certain PDN defects.



(a) 1-detect pattern set.

(b) Selected pattern set.

Figure 9: Transition fault and PDN defect coverage by different sets of patterns.

Considering the computation complexity, the run time needed for pattern sorting and selection is much less than that of potentially harmful open defects identification because other kinds of computation need neglectable time compared the time-consuming circuit simulation. For the similar reason, the time for defect identification is mainly dependent on the number of SCs in each segment since the proposed methodology needs to perform circuit simulation three times for each segment while the proposed voltage computation method consumes neglectable time compared to circuit simulation. In this experiment the average number of SCs inside each segment is 76, wherein the proposed methodology can reduce the computation time by 96%, compared to the case by circuit simulation only.

6. CONCLUSION AND FUTURE WORK

In this work, we propose novel techniques to identify potentially harmful open defects in the power distribution networks. To cover these defects, we also present an effective test pattern selection algorithm. Both methods can greatly reduce the time complexity. Experimental results show that our proposed techniques are able to result in high PDN defect coverage with the 1-detect transition fault patterns selected out of N-detect patterns, when compared to conventional 1-detect patterns.

Since a considerable part of the PDN defects cannot be detected by normal delay test patterns even after applying the test pattern selection technique presented in this work, we plan to work on ATPG techniques that are able to generate dedicated test patterns for PDN defects.

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