Yield Enhancement for 3D-Stacked ICs: Recent Advances and Challenges

Qiang Xu
CUhk REliable Computing Laboratory (CURE)
Dept. of Computer Science & Engineering
The Chinese University of Hong Kong
qxu@cse.cuhk.edu.hk

Li Jiang
CUhk REliable Computing Laboratory (CURE)
Dept. of Computer Science & Engineering
The Chinese University of Hong Kong
ljiang@cse.cuhk.edu.hk

Huiyun Li
Automotive Electronics Research Center
Shenzhen Institutes of Advanced Technologies
Chinese Academy of Sciences
hy.li@siat.ac.cn

Bill Eklow
Cisco Systems, Inc.
San Jose, CA
beklow@cisco.com

Abstract— Three-dimensional (3D) integrated circuits (ICs) that stack multiple dies vertically using through-silicon vias (TSVs) have gained wide interests of the semiconductor industry. The shift towards volume production of 3D-stacked ICs, however, requires their manufacturing yield to be commercially viable. Various techniques have been presented in the literature to address this important problem, including pre-bond testing techniques to tackle the "known good die" problem, TSV redundancy designs to provide defect-tolerance, and wafter/die matching solutions to improve the overall stack yield. In this paper, we survey recent advances in this filed and point out challenges to be resolved in the future.

I. Introduction

Three-dimensional (3D) technology that integrates multiple silicon dies with short and dense through-silicon vias (TSVs), being able to allow heterogeneous integration and provide abundant interconnect bandwidth with improved performance and less communication energy, has gained great interests of the semiconductor industry. Early 3D-stacked IC (3D-SIC) products for CMOS image sensor camera module were already in volume production [1]. 3D-stacked memory products were also announced by several companies [2–4]. In addition, more complicated 3D-SIC designs such as 3D NoC [5], 3D FPGA [6], 3D microprocessor [7], 3D cache and memory [8, 9], and memory-on-processor [10, 11] have been proposed to further exploit the benefits of this emerging technology. Moreover, aggressive 3D designs that employ a huge amount of TSVs were also under extensive research [12–14].

While 3D integration provides many benefits, such benefits can be realized only when the design and manufacturing cost of 3D-SIC products is commercially viable [15]. Among the various factors that affect 3D-SIC product cost, manufacturing yield is one of the most (if not the most) crucial ones [16], and it was showed that the functional yield of a rather simple 3-layer chip is only a bit more than 60% [17]. Generally speaking, there are two kinds of yield losses in 3D-SICs.

- *Stack yield loss*, caused by defects in one or more of the stacked dies. Generally speaking, there are three possible integration methods for 3D-SICs: wafer-to-wafer (W2W), die-to-wafer (D2W), or die-to-die (D2D) bonding. W2W bonding directly stacks wafers together and then dices them into individual die stacks. This bonding strategy leads to the highest throughput, but it requires that dies at different layers to have the same form factor, and thus, is suitable only for homogeneous integration (e.g. 3D-stacked memory). In addition, W2W integration may suffer from significant yield loss due to the stacking of good dies and bad dies, referred to as the "known good die" (KGD) issue. On the contrary, with D2W/D2D integration, bare dies are first diced from a wafer and then stacked to other dies/wafers. This bonding strategy facilitates to achieve higher stack yield than W2W bonding strategy, by only bonding those known good dies.
- *Assembly yield loss*, caused by defects occurred during the assembling process. The assembly process for 3D-SICs involves many challenging manufacturing steps (e.g., wafer thinning, handling and alignment), which may cause various types of TSV defects [18]. Before the bonding process, the wafer needs to be thinned first to expose the TSV tips at the back-side. Thus, it possibly leads to degradation of some I-V characteristics, shifts in device performances, and gives rise to yield losses [19, 20]. Insufficiently filling of TSVs is likely to occur during TSV fabrication process, which results in micro-voids inside TSVs. In [21], twelve different types of TSV defects were identified, eight of which involve defects that arise prior to bonding, while the rest is induced due to alignment, bonding, or stress. In addition, due to the inherent weakness on thermal dissipation, silicon devices composed of various materials in 3D stack with different coefficients of thermal expansion suffers from thermal-mechanical stress, and thus is prone to defect during stacking.

For stack yield improvement, needless to say, pre-bond testing plays an important role for D2W/D2D bonding and it is critical to achieve high defect coverage to prevent bad dies from being stacked [22]. Even for W2W bonding, with KGD information from pre-bond tests, stack yield improvement can be achieved by conducting selective wafer matching for maximal combination of good dies [23–26].

For assembly yield enhancement, adding redundant TSVs to repair faulty ones is probably the only effective method besides improving the manufacturing process itself. A number of TSV redundancy allocation strategies were presented in the literature and they differ in terms of redundancy ratio, repair flexibility and capability, and hardware cost (e.g., [27–29]).

Given the vast amount of research effort devoted to improve 3D-SIC yield, we present a comprehensive survey of related techniques in this paper. We first review the existing yield model for 3D-stacked ICs in Section II. Section III overviews recent advances of testing techniques for 3D-SICs. Then, we survey various wafer/die matching strategies for stack yield enhancement in Section IV. Next, TSV defect tolerance techniques for assemble yield enhancement are summarized in Section V. Finally, we present the challenges for further yield enhancement of 3D-SICs and point out some potential research directions.

II. Yield Modeling for 3D-Stacked ICs

The manufacturing yield of a single silicon die based on compound poisson model [30] is as follows:

$$Y_{die} = (1 + \frac{DA_{die}}{\alpha})^{-\alpha} \tag{1}$$

wherein D is the defect density, A_{die} is the die area and α is the clustering parameter related to the technology and the design itself (e.g., circuit density and mask steps).

Yield modeling for 3D-stacked ICs is more complicated considering the extra processing steps, various stacking manners, and the impact of die/wafer matching, as discussed in this section.

A. Stack Yield Modeling

Consider a 3D-SIC product containing N layers, and the yield of i^{th} layer die is Y_{die_i}. Its manufacturing yield using W2W integration (without matching) can be roughly calculated as follows:

$$Y_{stack,W2W} = \prod_{i=1}^{N}[Y_{die_i}] \tag{2}$$

With D2W/D2D integration, assuming perfect KGD tests, the yield of 3D-SIC product can be estimated as:

$$Y_{stack,D2W/D2D} = \min[Y_{die_i}], 1 \leq i \leq N \tag{3}$$

This is because, consider that we have the same number of dies fabricated for each layer, the final good die-stack will be constrained by the layer with the minimum number of good dies. The above clearly demonstrates the yield benefits of D2W/D2D integration [16, 22]. Let us now examine the yield model in detail considering the various factors besides bonding choice.

The impact of footprint: By partitioning a large monolithic 2D-IC into several smaller dies and stacking them together to provide the same functionality, it is in fact beneficial from the yield standpoint since each die now has a much smaller area. On the other hand, there is some additional area overhead for 3D-SICs with TSVs and design-for-testability (DfT) for pre-bond testing. We can roughly obtain the yield model for die i in 3D-SIC as follows:

$$Y_{die_i}^{3D} = (1 + \frac{D_i}{\alpha_i}(\frac{A_{die}^{2D}}{N} + O_i))^{-\alpha_i} \tag{4}$$

wherein A_{die}^{2D} is area of the monolithic 2D implementation and O_i is the extra area overhead of this particular die.

The impact of KGD test: As discussed earlier, pre-bond testing can be applied to identify known good dies for later bonding. Clearly, the test quality will affect the final yield of 3D-SIC products. The ratio of defective dies that escape pre-bond tests to all the ICs can be derived as [31]:

$$R_{escape} = 1 - Y_{die}^{1-F_c} \tag{5}$$

wherein F_c is the fault coverage of pre-bond tests. Thus, if D2W/D2D integration is used, the test escape ratio for the stacked IC can be estimated as [33]:

$$R_{escape,D2W/D2D} = 1 - \prod_{i=1}^{N} Y_{die_i}^{1-F_{c_i}} \tag{6}$$

Taking the above yield loss into consideration, the stack yield for D2W/D2D in Eq. 3 integration can be revised as:

$$Y_{stack,D2W/D2D} = \min[Y_{die_i}] \cdot \prod_{i=1}^{N} Y_{die_i}^{1-F_{c_i}} \tag{7}$$

The impact of wafer matching for W2W integration: In [32], Verbree *et al.* formulated a closed-form mathematical model to approximate the stack yield with wafer matching, by introducing a probability $p(j)$, which denotes the occurrence of matching exactly j faulty dies between two bonding wafers. There are some limitations in this analytical model, e.g., the model assumes a fixed number of faulty dies per stack tier, as pointed out in the paper itself.

B. Assembly Yield Modeling

The assembly yield ($Y_{assembly}$) of 3D-SIC products can be calculated as follows:

$$Y_{assembly} = Y_{Bonding} \cdot Y_{TSV} \tag{8}$$

wherein $Y_{Bonding}$ is the bonding yield and Y_{TSV} is the TSV yield [33]. Currently, there is still no concrete model for $Y_{Bonding}$ that takes device failure caused by bonding into account and it is typically assumed to be a constant value. For Y_{TSV}, as discussed earlier, TSVs are vulnerable to various kinds of defects introduced during fabrication and stacking process [22, 34]. Without redundancy, Y_{TSV} is simply:

$$Y_{TSV} = (1 - f_{TSV})^{N_{TSV}} \tag{9}$$

where f_{TSV} is the TSV failure rate and N_{TSV} is the total number of TSVs. From the above equation, TSV yield is a crucial factor for 3D-SIC products, especially when the number of TSVs are large and/or the TSV failure rate is high. Consequently, it is essential to incorporate redundancy for TSV defect-tolerance.

C. Cumulative Yield Model

According to the cumulative yield property [35], the final yield of 3D-stacked SICs Y_{final} can be formulated as follows:

$$Y_{final} = Y_{stack} \prod_{i=1}^{N-1} Y_{assembly(i)} \quad (10)$$

where N is the number of layers in the 3D-stacked IC product, Y_{stack} is the stacking yield and $Y_{assembly(i)}$ is the assembly yield for the i^th assembly process.

With the various factors that affect the final yield of 3D-SIC products introduced above, we discuss yield enhancement techniques in the following sections.

III. Design for Pre-Bond Testability

Despite the fact that there were lots of optimization works to reduce the test cost of 3D-SICs (e.g., [36, 37]), we mainly focus on the testability issues for pre-bond testing[1] in this section because they determine the possible test coverage of each individual die, which in turn affect the final yield of 3D-SICs.

One of the earliest works that address the testability issues of 3D-SICs is by Lewis and Lee [39]. In this work, the authors considered testing 3D-SICs with fine-grained circuit-level partitioning (i.e., functional blocks spread across multiple dies) and proposed a "scan island" approach to test incomplete circuits. While practically speaking, it is unlikely to have 3D-SIC products with fine-grained partitioning in the foreseeable future, this work pointed out two important observations: i) test access is the key challenge in pre-bond testing due to difficult probing; ii) it is essential to provide test infrastructure support for effective pre-bond testing. Extensive research efforts have been made to tackle the above issues.

A. Wafer Probing

It is extremely difficult, if not impossible, to probe TSVs directly due to their tiny sizes. Consequently, a number of dedicated test pads usually need to be fabricated on silicon die so that automatic test equipment (ATE) can access them during testing, and they occupy much larger area (when compared to TSVs) according to the footprint of probe needles. Also, care must be taken so that the probe force on thinned wafer would not damage the wafer itself [22]. To migrate these challenges, we have to constrain the number of test pads used for pre-bond testing [40]. Recently, Noia and Chakrabarty [41] developed novel DfT structures that allows multiple TSVs to be touched by the same probe-head, thus hiding the pitch gap between probe needle and TSVs.

Due to its unique advantage to enable contactless testing, wireless probing seems to be a perfect solution for pre-bond testing and it has attracted lots of research interests [42–44]. In this technique, micro antennas need to be implemented in the circuit under test and they communicate with the wireless tester [45] via capacitive coupling. In order to support wireless wafer-level test without adding test pads, power supply also needs to be realized using wireless DC voltage transmission technique [46]. While the concept of wireless probing is attractive and there has been some research progress in this area, it is still a long way to go for this technique to be adopted in practice.

[1]Besides testing individual dies before the bonding process, the test cost analysis work [38] also discussed the impact of conducting "intermediate stack test" and "pre-package test" before the final post-bond package test, and they are treated as part of pre-bond testing in this paper.

B. Design for Test Access

Lewis *et al.* [47] proposed several test methods for circuit-level partitioned 3D-SICs. The basic strategy is to establish the control-observe points, by either inserting scan registers to support structural test or selectively partitioning a functional block so that the read/write ports are both available on the same layer so as to use functional test. Instead of inserting scan flip-flops to both ends of TSVs, [48] proposed to reuse existing primary I/Os or pseudo primary I/Os to provide controllability and observability for signals associated with TSVs. Wu *et al.* [49] proposed 3D scan chain design that cross multiple dies to minimize the stitching wirelength.

For the more practical 3D-SICs partitioned at block or core level, modular testing is a natural choice to reduce the required number of test pads. Marinissen *et al.* [50] proposed to add IEEE 1500-like test wrapper for a die with 3D-specific extensions, such as dedicated test pads for pre-bond probing. In [51], the proposed die-level wrapper is extended to IEEE 1149.1 by providing external control interface, which is being formalized as IEEE P1838 standard [52]. With reconfigurable wrapper instruction registers, this technique can be further extended to support 2.5-D integration, wherein one layer actually contains multiple dies, referred as "multiple towers" [53], which requires a scalable test mechanism and wrapper configuration for both pre-bond test and post-bond test.

C. Test Infrastructure Design

Besides difficult test access to circuit I/Os, pre-bond testing also poses unique challenges for the supporting test infrastructure design such as power supply delivery and clock network. That is, we may not have a fully-connected 2D clock tree on each die and require a large number of test pads for clock signals and power/ground connection, without considering pre-bond testability up front in the design flow.

Zhao *et al.* proposed to synthesize clock tree for pre-bond testability in [54], which tries to minimizes the overall wirelength and clock power consumption under given skew and slew constraints. This work was later improved in [55], which significantly reduced clock power and used much less TSVs. Panth and Lim [56] studied the power delivery network for pre-bond test of 3D ICs. Their proposed method on adding probe pads is able to take the impact of TSVs on power/voltage drop into consideration.

D. Pre-bond TSV Testing

As discussed earlier, various types of TSV defects are introduced before the bonding process [21], and it is certainly beneficial to identify them during pre-bond testing to improve the stack yield of 3D-SICs.

Since TSV defects would affect the electrical behavior of circuits connecting to the TSV (e.g., the sense-amplifier in 3D-DRAM [57]), a natural method to test TSVs prior to bonding is to measure the I-V characteristics (e.g., resistance and capacitance) with the help of DfT circuitries built around TSV endpoints. The application of on-chip sense amplification was proposed in [58, 62] for detecting capacitive TSV faults. Futher, a voltage divider is added for scannable voltage test [59]. Two other methods utilizing leakage current sensor and capacitive bridge were evaluated in [60] to measure TSV resistance and capacitance. The accuracy of the above techniques is quite sensitive to the tester capability and environmental noises. [61] proposed on-chip test circuits that are less immune to the above effects.

IV. Wafer/Die Matching for Yield Enhancement

With KGD information acquired from pre-bond testing, we can apply wafer matching to improve the stack yield of 3D-SICs with W2W integration, by avoiding to stack good and bad dies together, whenever possible. For 3D-SICs containing only two layers, this problem can be formulated as a maximum weight bipartite graph matching problem [16] and use well-known algorithm to solve it in polynomial time [63]. For 3D-SICs containing three or more layers, however, one can prove that maximizing their yield via wafer matching is a NP-hard problem, by reducing the classical NP-hard 3D matching problem [64] to it. Reda *et al.* [23] hence proposed a heuristic based on Hungarian algorithm [63] to solve this problem. Verbree *et al.* [32] conducted extensive simulation for a larger number of wafers with hypothetical faulty maps, which shows that the expected yield is deeply influenced by *matching parameters* such as the number of stack layers, the number of dies per wafer, and the wafer repository size. In particular, a larger wafer repository enlarges the solution space of the matching algorithm, and thus facilitates to find more good wafer pairs. To investigate the impact of replenished repositories where the wafer repository size decreases as matching conducts, Taouil *et al.* [65] discussed various matching scenarios that are suitable for such running repository.

While wafer matching is helpful for stack yield improvement, its effectiveness is fundamentally constrained by the defect rate of individual dies, unless there is some remedy to make use of bad dies after stacking. This is possible for 3D-stacked memory circuits with the help of inter-die redundancy sharing schemes [24, 25]. In particular, [25] showed great stack yield improvement with two-dimensional redundancy for inter-die memory repair.

With the ever-increasing process variation effects with technology scaling, the performance and power consumption of functional dies can be quite different. Wafer/die matching can be utilized to mitigate such effects. Ferri *et al.* [26] proposed to use maximum matching algorithm for parametric yield enhancement for a CPU-to-L2 cache die stack, considering the variation of operational frequency of CPU and access latency of L2 cache.

V. Defect Tolerance for TSV Failures

TSV failure rates can vary significantly among different 3D-SIC designs because the failure rate of a particular technology depends on its technology maturity level and parameters such as TSV width/height and TSV pitch size. The common belief is that: while the TSV processing technology has advanced significantly over the past several years, TSV yield is still not satisfactory, requiring to add redundancy for defect-tolerance, especially for those 3D-SIC designs that employ massive use of TSVs (e.g.[5, 12–14]).

In [2], Samsung presented the TSV redundancy strategy used to improve the yield of its 3D memory product composed of four tiers connected by roughly 300 TSVs (see Fig. 1(a)). Six TSVs are bundled as a group, including four signal TSVs and two spare ones. The redundancy ratio is therefore 1:2 and it can tolerate any one or two TSV failures within a group.

A chain of multiplexors is employed in [27] to link signal TSVs with one spare one as a TSV-chain (see Fig. 1(b)). When the chain contains one defective TSV, the signals transmitted on it and on all subsequent TSVs of the chain are shifted to other good TSVs. Suppose each TSV block contains N TSVs, the redundancy ratio of this technique is $1 : N$. This technique can repair only one defective TSV in each group, suitable for 3D-SICs that employ large-sized TSVs (and hence with low vulnerability).

Loi *et al.* [66] proposed a defect-tolerance technique for 3D network-on-chip links. In this technique, for a TSV grid used as NoC links, redundant TSVs are added to each row or column and they are connected to the signal TSVs on the same row/column through a crossbar (see Fig. 1(c)). Consequently, the signal connecting to a defective TSV can be routed to a redundant one for repair, if any. Consider a $N \times N$ TSV grid[2], the redundancy ratio of this technique is $1 : N$, and it can tolerate any single TSV failure in each row/column in the grid.

Despite the different redundancy allocation strategies used in these works, they all assume uniformly-distributed TSV faults and use neighboring TSVs to replace faulty ones, if any. In practice, however, the bonding quality of TSVs depends on not only the bonding technology, but also the winding level of the thinned wafer and the surface roughness and cleanness of silicon dies. Consequently, if one TSV is defective during the bonding process, it is more likely that its neighboring TSVs are also faulty. Due to such clustering effect, earlier TSV repair techniques are less effective because a signal TSV and its neighboring redundant one may be defective at the same time. To address this problem, Jiang *et al.* [28] presented a novel TSV repair framework that enables faulty TSVs to be repaired by spares that are distant with the help of simple routers (see Fig. 1(d)).

VI. Challenges and Future Research Direction

While a large amount of research effort has been devoted to improve the manufacturing yield of 3D-SICs, as discussed in this paper, there are still many challenging problems to be resolved in the future to make 3D-SICs to become mainstream products.

[2]Due to the area cost of the crossbar design, N cannot be a large value.

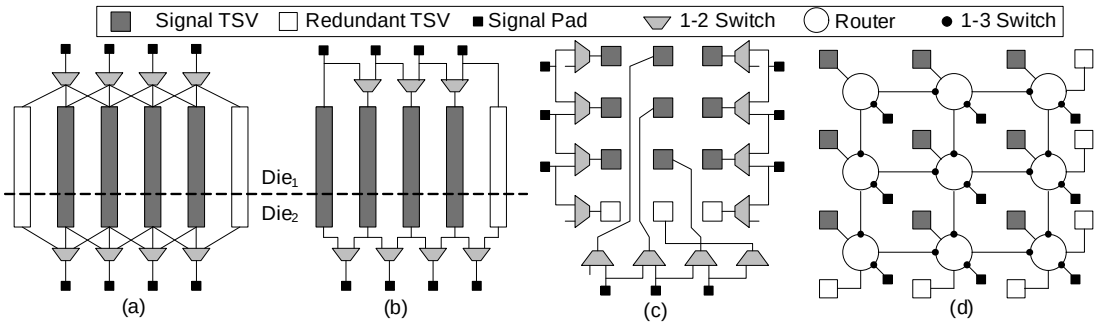

Fig. 1. TSV Redundancy Allocation Schemes: (a) Signal-Switching [2], (b) Signal-Shifting [27], (c) Crossbar [66], (d) Router [28]

The current yield model for 3D-stacked ICs is still quite immature. In particular, the impact of wafer/die matching on the final yield of 3D-SICs is overly simplified in the current yield model. In addition, the defect density of thinned wafer could be quite different from conventional wafer and has not been studied in the literature. Moreover, the yield loss caused by the bonding process is unclear and needs further research, which should take the impact of TSV stress on neighboring devices and alignment issues into consideration.

While extensive works have been conducted to understand new types of defects introduced in 3D integration and a majority of them can be covered by conventional fault models, there is little work discussing the clustering faulty effect in 3D-SICs. It is essential to study this phenomenon in future research because it significantly affects the effectiveness of TSV redundancy design and hence assembly yield of 3D-SICs. In addition, TSV coupling capacitance may not be ignorable [57, 68] and such effects deserves further research, especially for future 3D-SICs that employ a large amount of TSVs.

Wafer probing and effective KGD test remain to be one of the most critical challenges, which in turn affect the stack yield of 3D-SICs. While there have been some DfT techniques proposed to address these issues, they typically involve non-trivial design cost and require long testing time to perform. Some of the known solutions also have simplified assumptions. For example, modular test access design is limited by the assumption that all the devices are scan testable. It is necessary to consider more complicated scenarios, e.g., clock generator, analog/RF and non-CMOS devices. Consequently, novel DfT designs and test strategies (in particular, built-in self-test solutions that require less test pads) to improve the cost-effectiveness of prebond testing desperately needs further research.

Existing TSV redundancy allocation strategies are still far from satisfactory, requiring high redundancy ratio to achieve acceptable assembly yield. Even though latest technique such as [28] is able to deal with clustering TSV failures, the repair efficiency can be still low since spare TSVs can only be used to replace defective ones within a group determined a priori [29]. Future research should consider to allow spare TSVs to be reconfigured to repair defective ones in multiple groups under timing constraints, thus greatly improving repair efficiency.

Last but not least, it is always beneficial to consider the yield issue up front in the design flow. For example, a poor system partition may lead to low yield of dies on certain layer and more irregular TSV placement, which is hardly offset by later yield enhancement techniques.

VII. Acknowledgements

This work was supported in part by a research grant from Cisco Systems.

References

[1] V. Suntharalingam, et al., "Megapixel CMOS image sensor fabricated in three-dimensional integrated circuit technology," In *Proc. IEEE International Solid-State Circuits Conference*, pp. 356–357, 2005.

[2] U. Kang, et al., "8 Gb 3-D DDR3 DRAM using through-silicon-via technology," *IEEE Journal of Solid-State Circuits*, 45(1):111–119, 2010.

[3] T. Mitsuhashi, et al., "Development of 3-D-packaging process technology for stacked memory chips," In *Proc. IEEE International 3D Systems Integration Conference*, pp. 155–162, 2006.

[4] M. Kawano, et al., "A 3D packaging technology for 4 Gbit stacked DRAM with 3 Gbps data transfer," In *Proc. IEEE International Electron Devices Meeting*, pp. 1–4, 2006.

[5] B. S. Feero and P. P. Pande, "Networks-on-chip in a three-dimensional environment: A performance evaluation," *IEEE Transactions on Computers*, 58(1):32–45, Jan. 2009.

[6] C. Ababei, P. Maidee, and K. Bazargan, "Exploring potential benefits of 3D FPGA integration," *Field Programmable Logic and Application*, pp. 874–880, 2004.

[7] G. H. Loh, Y. Xie, and B. Black, "Processor design in 3D die-stacking technologies," *IEEE Micro*, 27(3):31–48, May-June 2007.

[8] K. Puttaswamy and G. H. Loh, "3D-integrated SRAM components for high-performance microprocessors," *IEEE Transactions on Computers*, 58(10):1369–1381, 2009.

[9] Y.F. Tsai, et al., "Design space exploration for 3-D cache," *IEEE Transactions on VLSI Systems*, 16(4):444–455, 2008.

[10] R.S. Patti, "Three-dimensional integrated circuits and the future of system-on-chip designs," *Proceedings of the IEEE*, 94(6):1214–1224, June 2006.

[11] F. Li, et al., "Design and management of 3D chip multiprocessors using network-in-memory," In *Proc. International Symposium on Computer Architecture*, pp. 130–141, 2006.

[12] J. H. Chien, et al., "Floorplanning 1024 cores in a 3D-stacked network-on-chip with thermal-aware redistribution," In *Proc. Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems*, pp. 1–6, 2010.

[13] G.H. Loh, "3D-stacked memory architectures for multi-core processors," In *Proc. International Symposium on Computer Architecture*, pp. 453–464, 2008.

[14] H. W. Dong, N. H. Seong, D. L. Lewis, and H.-H. S. Lee, "An optimized 3D-stacked memory architecture by exploiting excessive, high-density TSV bandwidth," In *Proc. IEEE International Symposium on High Performance Computer Architecture*, pp. 1–12, 2010.

[15] X. Dong and Y. Xie, "System-level cost analysis and design exploration for three-dimensional integrated circuits (3D ICs)," In *Proc. IEEE Asia South Pacific Design Automation Conference*, pp. 234–241, 2009.

[16] G. Smith, L. Smith, S. Hosali, and S. Arkalgud, "Yield considerations in the choice of 3D technology," In *Proc. International Symposium on Semiconductor Manufacturing*, pp. 1–3, 2007.

[17] N. Miyakawa, "A 3D prototyping chip based on a wafer-level stacking technology," In *Proc. IEEE Asia South Pacific Design Automation Conference*, pp. 416–420, 2009.

[18] J. U. Knickerbocker, et al., "Three-dimensional silicon integration," *IBM Journal of Research and Development*, 52(6):553–569, Nov. 2008.

[19] A. Ikeda, et al., "Design and measurements of test element group wafer thinned to 10um for 3D system in package," In *Proc. IEEE International Conference on Microelectronic Test Structures*, pp. 161–164, 2004.

[20] Dan Perry et al., "Impact of thinning and packaging on a deep sub-micron CMOS product," In *Digest of DATE Workshop on 3D Integration*, page 282, 2009.

[21] C.-N. Peng, et al., "Electrical tests for three-dimensional ICs (3DICs) with TSVs," *International Test Conference 3D-Test Workshop*, 2010.

[22] H.-H. S. Lee and K. Chakrabarty, "Test challenges for 3D integrated circuits," *IEEE Design & Test of Computers*, 26(5):26–35, Sept.-Oct. 2009.

[23] S. Reda, G. Smith, and L. Smith. Maximizing the functional yield of wafer-to-wafer 3-D integration. *IEEE Transactions on VLSI Systems*, 17(9):1357–1362, Sept. 2009.

[24] C. W. Chou, Y. J. Huang, and J. F. Li, "Yield-enhancement techniques for 3D random access memories," In *Proc. International Symposium on VLSI Design Automation and Test*, pp. 104–107, 2010.

[25] L. Jiang, R. Ye, and Q. Xu, "Yield enhancement for 3D-stacked memory by redundancy sharing across dies," In *Proc. International Conference on Computer-Aided Design*, pp. 230–234, 2010.

[26] C. Ferri, S. Reda, and R. I. Bahar, "Parametric yield management for 3D ICs," *ACM Journal on Emerging Technologies in Computing Systems*, 4(4):19:1–19:22, Oct. 2008.

[27] A. C. Hsieh, et al., "TSV redundancy: Architecture and design issues in 3D IC," In *Proc. IEEE/ACM Design, Automation, and Test in Europe*, pp. 166–171, 2010.

[28] L. Jiang, Q. Xu, and B. Eklow, "On effective TSV repair for 3D-stacked ICs," In *Proc. IEEE/ACM Design, Automation, and Test in Europe*, to appear, 2012.

[29] Y. Zhao, S. Khursheed, and B. Al-Hashimi, "Cost-effective TSV grouping for yield improvement of 3D-ICs," In *Proc. IEEE Asian Test Symposium*, 2011.

[30] I. Koren and Z. Koren, "Defect tolerance in VLSI circuits: techniques and yield analysis," *Proceedings of the IEEE*, 86(9):1819–1838, 1998.

[31] T.W. Williams and N.C. Brown, "Defect level as a function of fault coverage," *IEEE Transactions on Computers*, C-30(12):987–988, Dec. 1981.

[32] J. Verbree, E. J. Marinissen, P. Roussel, and D. Velenis, "On the cost-effectiveness of matching repositories of pre-tested wafers for wafer-to-wafer 3D chip stacking," In *Proc. IEEE European Test Symposium*, pp. 36–41, 2010.

[33] Y. Chen, D. Niu, Y. Xie, and K. Chakrabarty, "Cost-effective integration of three-dimensional (3D) ICs emphasizing testing cost analysis," In *Proc. International Conference on Computer-Aided Design*, pp. 471–476, 2010.

[34] E.J. Marinissen and Y. Zorian, "Testing 3D chips containing through-silicon vias," In *Proc. IEEE International Test Conference*, pp. 1–11, 2009.

[35] Y. Deng and W.P. Maly, "2.5-dimensional VLSI system integration," *IEEE Transactions on VLSI Systems*, 13(6):668–677, June 2005.

[36] L. Jiang, L. Huang, and Q. Xu, "Test architecture design and optimization for three-dimensional SoCs," In *Proc. IEEE/ACM Design, Automation, and Test in Europe*, pp. 220–225, 2009.

[37] B. Noia, K. Chakrabarty, and Y. Xie, "Test-wrapper optimization for embedded cores in TSV-based three-dimensional SOCs," In *Proc. IEEE International Conference on Computer Design*, pp. 70–77, 2009.

[38] M. Taouil, S. Hamdioui, K. Beenakker, and E. J. Marinissen, "Test cost analysis for 3D die-to-wafer stacking," In *Proc. IEEE Asian Test Symposium*, pp. 435–441, 2010.

[39] D. L. Lewis and H.-H. S. Lee, "A scan-island based design enabling pre-bond testability in die-stacked microprocessors," In *Proc. IEEE International Test Conference*, paper 21.2, 2007.

[40] L. Jiang, Q. Xu, K. Chakrabarty, and T. M. Mak, "Layout-driven test-architecture design and optimization for 3D SoCs under pre-bond test-pin-count constraint," In *Proc. IEEE/ACM International Conference on Computer-Aided Design*, pp. 191–196, 2009.

[41] B. Noia and K. Chakrabarty, "Pre-bond probing of TSVs in 3D stacked ICs," In *Proc. IEEE International Test Conference*, 2011.

[42] D. Saltzman and T. Knight, "Capacitive coupling solves the known good die problem," In *Proc. IEEE Multi-Chip Module Conference*, pp. 95–100, 1994.

[43] G.-S. Kim, et al., "A high-speed, low-power capacitive-coupling transceiver for wireless wafer-level testing systems," In *Proc. IEEE International 3D Systems Integration Conference*, pp. 1–4, 2010.

[44] C. V. Sellathamby, et al., "Noncontact wafer probe using wireless probe cards," In *Proc. IEEE International Test Conference*, paper 18.3, 2005.

[45] C.-W. Wu, et al., "The HOY tester - can IC testing go wireless?" In *Proc. IEEE International Symposium on VLSI Design, Automation and Test*, pp. 1–4, 2006.

[46] Y. Yoshida, et al., "Wireless DC voltage transmission using inductive-coupling channelfor highly-parallel wafer-level testing," In *Proc. IEEE International Solid State Circuits Conference*, pp. 470–471, 2009.

[47] D. L. Lewis and H.-H. S. Lee, "Testing circuit-partitioned 3D IC designs," In *Proc. IEEE Computer Society Annual Symposium on VLSI*, pp. 139–144, 2009.

[48] J. Li and D. Xiang, "DfT optimization for pre-bond testing of 3D-SICs containing TSVs," In *Proc. International Conference on Computer Design*, pp. 474–479, 2010.

[49] X. Wu, P. Falkenstern, and Y. Xie, "Scan chain design for three-dimensional integrated circuits (3D ICs)," In *Proc. IEEE International Conference on Computer Design*, pp. 208–214, 2007.

[50] E. J. Marinissen, J. Verbree, and M. Konijnenburg, "A structured and scalable test access architecture for TSV-based 3D stacked ICs," In *Proc. IEEE VLSI Test Symposium*, pp. 269–274, 2010.

[51] E. J. Marinissen, C.-C. Chi, J. Verbree, and M. Konijnenburg, "3D DfT architecture for pre-bond and post-bond testing," In *Proc. IEEE International 3D Systems Integration Conference*, pp. 1–8, 2010.

[52] Test access architecture for three-dimensional stacked integrated circuits.proposed IEEE standard P1838.

[53] C.-C. Chi, E. J. Marinissen, S. K. Goel, and C.-W. Wu, "DfT architecture for 3D-SICs with multiple towers," In *Proc. IEEE European Test Symposium*, pp. 51–56, 2011.

[54] X. Zhao, D. L. Lewis, H. H. S. Lee, and S. K. Lim, "Pre-bond testable low-power clock tree design for 3D stacked ICs," In *Proc. IEEE/ACM International Conference on Computer-Aided Design*, pp. 184–190, 2009.

[55] T.-Y. Kim and T. Kim, "Clock tree synthesis with pre-bond testability for 3D stacked IC sesigns," In *Proc. IEEE/ACM Design Automation Conference*, pp. 723–728, 2010.

[56] S. Panth and S. K. Lim, "Scan chain and power delivery network synthesis for pre-bond test of 3D ICs," In *Proc. IEEE VLSI Test Symposium*, pp. 26–31, 2011.

[57] L. Jiang, et al., "Modeling TSV open defects in 3D-stacked DRAM," In *Proc. IEEE International Test Conference*, paper 6.1, 2010.

[58] P.-Y. Chen, C.-W. Wu and D.-M. Kwai, "On-chip TSV testing for 3D IC before bonding using sense amplification," In *Proc. IEEE Asian Test Symposium*, pp. 450–455, 2009.

[59] M. Cho, et al., "Design method and test structure to characterize and repair TSV defect induced signal degradation in 3D system," In *Proc. IEEE/ACM International Conference on Computer-Aided Design*, pp. 3–6, 2010.

[60] F. Zhang, Y. Lou, Z. Yan and P. Franzon, "Comparing through-silicon-via (TSV) void/pinhole defect self-test methods," In *International Test Conference 3D-Test Workshop*, 2010.

[61] M. Cho, et al., "Pre-bond and post-bond test and signal recovery structure to characterize and repair TSV defect induced signal degradation in 3-D system," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, (99):1–10, 2011.

[62] P.-Y. Chen, C.-W. Wu, and D.-M. Kwai, "On-chip testing of blind and open-sleeve TSVs for 3D IC before bonding," In *Proc. IEEE VLSI Test Symposium*, pp. 263–268, 2010.

[63] J. Munkres, "Algorithms for the assignment and transportation problems," *Journal of the Society for Industrial and Applied Mathematics*, pp. 32–38, 1957.

[64] M. R.Garey and D. S.Johnsonand ed., *Computers and Intractability: A Guide to the Theory of NP-Completeness*. W.H. Freeman and Company, 1979.

[65] M. Taouil, S. Hamdioui, J. Verbree, and E.J. Marinissen, "On maximizing the compound yield for 3D wafer-to-wafer stacked ICs," In *Proc. IEEE International Test Conference*, paper 6.2, 2010.

[66] I. Loi, et al., "A low-overhead fault tolerance scheme for TSV-based 3D network on chip links," In *Proc. IEEE/ACM International Conference on Computer-Aided Design*, pp. 598–602, 2008.

[67] H. L. Leong, et al., "Effects of applied loads, effective contact area and surface roughness on the dicing yield of 3D Cu bonded interconnects," *Technology*, (c):4–6, 2006.

[68] I. Savidis and E. G. Friedman, "Closed-form expressions of 3-D via resistance, inductance, and capacitance," *IEEE Transactions on Electron Devices*, 56(9):1873–1881, 2009.