

On the Simulation of NBTI-Induced Performance Degradation Considering Arbitrary Temperature and Voltage Variations

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ABSTRACT

With aggressive CMOS technology scaling, Negative Bias Temperature Instability (NBTI) has emerged as one of the major system lifetime reliability threats, which gradually increases PMOS transistor threshold voltage and hence results in increased circuit delay. NBTI-induced performance degradation depends heavily on time-varying parameters such as temperature, duty cycle and supply voltage. Previous analytical models for NBTI effects, however, cannot cover all these parameters, causing overly optimistic or overly pessimistic analysis. In this work, we propose a comprehensive NBTI analytical model that explicitly takes supply voltage, duty cycle and temperature variations into consideration. The accuracy of the proposed model is validated against cycle-accurate simulation for NBTI effects. In addition, based on the proposed model, we present an efficient simulation framework for system lifetime prediction by running representative workloads only. Experimental results demonstrate the efficacy and efficiency of the proposed solution.

1. INTRODUCTION

With continuous scaling of CMOS technology, we are able to integrate more functionalities with improved performance onto a single silicon die in each new technology generation. At the same time, however, integrated circuits suffer from ever-increasingly severe reliability threats such as Electromigration (EM) [1], Hot Carrier Injection (HCI) [2], and Negative Bias Temperature Instability (NBTI) [3]. Among all the circuit failure mechanisms, NBTI has become a major system lifetime reliability threat since 90nm technology [4] and gets even worse with further scaling. NBTI manifests itself as the gradual increase of threshold voltage of the PMOS transistor, which increases circuit delay and eventually results in circuit timing violations. As pointed out in [7], NBTI may degrade circuit speed for up to 20% with 10 years operation.

NBTI occurs due to the generation of the interface traps at the $Si - SiO_2$ interface when PMOS transistors are biased with negative voltage (e.g., when $V_{gs} = -V_{dd}$). The degradation effects can be partially recovered after the removal of stress voltage (e.g., when $V_{gs} = 0$). Therefore, the effect of

NBTI on PMOS depends on the amount of time the transistor has been stressed and relaxed. The more time PMOS under stress condition, the more degradation it experiences. NBTI is also highly sensitive to operating temperature. Higher temperature can accelerate the generation of interface traps and thus exacerbates performance degradation. In [5], the authors showed that threshold voltage shift can increase up to 42% at high temperature. In addition to stress probability and temperature, supply voltage is also a major factor contributing to NBTI degradation.

A significant amount of research efforts have been dedicated to modeling NBTI-induced performance degradation [6, 7, 9–13]. Since NBTI is a complex failure mechanism that involves many time-varying factors (e.g., temperature, stress probability and supply voltage), for the sake of simplicity, previous works often assume constant values for one or more of these parameters. Consequently, aging analysis and prediction based on these models can be quite inaccurate. Accurate NBTI-induced degradation model (i.e., cycle-accurate model [8]), however, is inefficient for long term estimation (e.g., lifetime reliability). To tackle the above problem, in this paper, we develop an accurate yet efficient simulation framework for NBTI-induced performance degradation. The major contributions of this work include:

- We develop a comprehensive NBTI analytical model that takes all the time-varying parameters related to NBTI degradation into consideration. To be specific, in the proposed model, we use a single parameter, degradation rate, to cover time-independent factors of NBTI degradation, which enables us to compute the degradation at any specific time of system's service life.
- We present a novel simulation framework that can efficiently estimate NBTI-induced system lifetime. Our framework does not require to trace NBTI-related factors over its entire lifetime. Instead, we run representative workloads on the system once and then compute NBTI-induced degradation rate based on the traced information. System lifetime can then be estimated accurately and efficiently with our framework.

The rest of the paper is organized as follows. In Section 2, we review prior research and motivate this work. Section 3 describes PCPs degradation and the simulation framework. Section 4 presents the proposed NBTI analytical model. Experimental results are then presented in Section 5. Finally, Section 6 concludes this paper.

2. RELATED WORK AND MOTIVATION

NBTI analytical models usually base on Reaction-Diffusion (R-D) mechanism. In [9], the authors proposed an analytical

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model for NBTI and showed NBTI effects are independent of circuit operational frequency. Cycle-accurate and long-term degradation models were presented in [10]. According to these models, long-term NBTI threshold voltage degradation is often approximated as $\Delta V_{th} = At^n$, where A is related to both device parameters (e.g., gate oxide thickness) and operational parameters (e.g., duty cycle, temperature and supply voltage).

In order to obtain A , prior works often assume constant temperature and supply voltage when predicting NBTI-induced performance degradation (usually consider the worst-case scenario to be safe). In practice, these operational parameters may vary significantly with different workloads. For example, [14] showed that temperature can vary up to 50°C for today’s high-performance microprocessors. Moreover, in order to achieve better energy-performance tradeoff, state-of-the-art integrated circuits are essentially adaptive systems, i.e., they would adjust runtime behaviors based on performance requirements. For example, dynamic voltage and frequency scaling (DVFS) is widely-used in modern processors for energy savings. Consequently, those analytical models that assume constant temperature and supply voltage values would result in significant errors. [12, 13] presented temperature-aware analytical models for NBTI effects, but they only consider two temperature values, for active and standby modes, respectively. A compact NBTI model that can handle arbitrary temperature variation was proposed in [11], but it does not consider supply voltage variations. [16, 17] proposed logarithmic NBTI models by considering dynamic voltage scaling, but they do not cover the impact of temperature variations. In one word, for NBTI-induced degradation, *the device stresses in different time intervals are not additive* [8], and therefore it is inaccurate for the above models to accumulate the NBTI-induced degradation along time axis, by fixing one of the time-varying factors (either temperature or voltage/frequency). [8] proposed an analytical model for NBTI degradation considering temperature and voltage variations, but the degradation has to be computed cycle by cycle, which is not practical for long-term degradation analysis.

From the above, it is important to simulate the actual workloads running on the system to obtain accurate long-term NBTI-induced degradation effects. However, it is impossible to simulate the entire service life of a system with various types of workloads. To mitigate this problem, in [15], the authors proposed a novel simulation framework, namely *AgeSim*, to estimate system lifetime by running representative workloads only (see Fig. 1). When running the representative workloads, the reliability-related usage strategies (e.g., various dynamic power management policies and various dynamic voltage and frequency scaling techniques) determine the system’s execution state. Then, *AgeSim* uses a scale parameter ($\Theta(T_i, S_i)$) to cover the state-related parameters (voltage and frequency), which builds a linear relationship between aging effect and time t . Thus, *AgeSim* can accumulate $\Theta(T_i, S_i)$ within the limited representative workloads and extract a time-independent factor, namely Aging Rate (Ω). As long as the characteristic of the representative workloads is consistent with that of entire lifetime, the derived Ω can be used to estimate system’s reliability at any time t .

The high-level lifetime reliability models presented in [15], however, cannot be used for analyzing NBTI-induced performance degradation, because of the following reasons: (a) *NBTI-induced degradation is not additive along time axis* [8], and therefore accumulating individual degradation from separate time units leads to inaccurate estimation of the long-term degradation; (b) The state-related scale parameter $\Theta(T_i, S_i)$ is difficult to calculate for individual devices, like PMOS transistor, and therefore is only applicable for statistical analysis

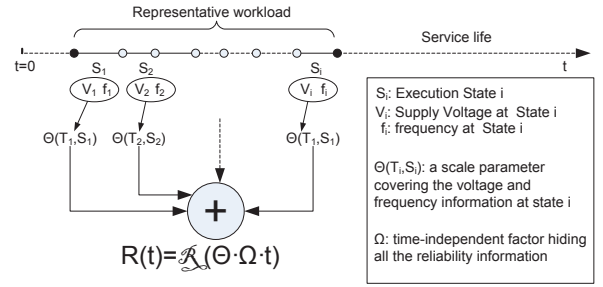


Figure 1: The reliability model in *AgeSim* [15]

of failure mechanisms, in which scale parameter has a simple relation with Mean-Time-To-Failure under the assumption of Weibull distribution; (c) *AgeSim* does not take circuit structure into consideration, while NBTI effects are strongly related to circuit structure as they would only affect critical paths or near-critical paths, denoted as potential critical paths (PCPs) in this paper.

Motivated by the above, in this work, we present a comprehensive analytical model and the corresponding simulation framework for NBTI-induced performance degradation. To the best of our knowledge, it is the first analytical model that explicitly considers arbitrary temperature and supply voltage variations for simulation of long-term NBTI effects, as detailed in the following sections.

3. THE PROPOSED SIMULATION FRAMEWORK

In order to efficiently estimate system lifetime, we run representative workloads on the system and trace NBTI-related reliability parameters during the simulation. The traced information is used to calculate NBTI-induced degradation rate Ω . As long as the usage strategy of the representative period is consistent of system’s service life, we can use degradation rate Ω to predict NBTI-induced degradation at any time t of its service lifetime. Unlike [15], wherein the aging rate Ω represents a high level aging effect, in this work, we propose to extract the NBTI-induced degradation rate at transistor level considering various runtime parameters variations, and estimate the long term NBTI-induced delay degradation of a PMOS transistor based on it. After deriving the above delay degradation, we take into account the circuit structure to estimate the long-term delay degradation of the whole system. Before detailing how to derive such a variation-aware NBTI model at transistor level (see Section 4), let us present the overall NBTI-induced lifetime reliability simulation framework in this section.

Fig. 2 shows the simulation flow to estimate NBTI-induced performance degradation. When running the representative workloads, DPM and/or DVFS determine processor’s execution states (supply voltage and frequency). We first trace the supply voltage/frequency in each state. We assume all the PMOS transistors have the same voltage/frequency at any time t . We further trace the power consumption for temperature simulator (e.g., HotSpot) to obtain temperature distributions in each states. We cannot afford to trace the temperature information for each PMOS transistor. Thus, we divide the system into several functional blocks (such as registers, ALUs, caches and etc.), and assume PMOS transistors in the same block has the same temperature distribution. If the block is too large, we can further divide it into smaller ones so that temperature variations in the same block can be ignored. At last, the timing analysis tool is used to trace the duty cycles of each PMOS transistor from the representative workloads. With the above traced time-varying information (i.e., duty cycle, temperature, supply voltage and frequency), we can compute the

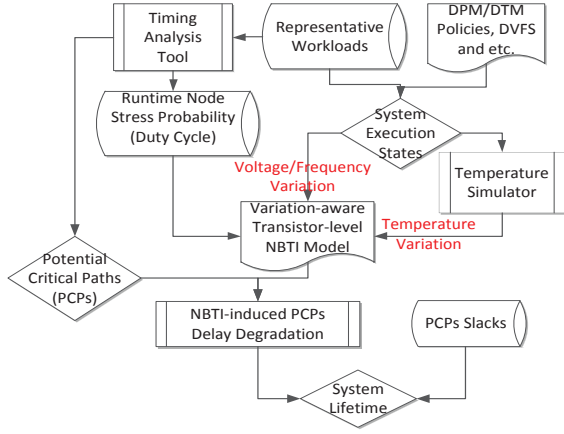


Figure 2: Proposed Simulation Framework for NBTI-aware System Lifetime Estimation.

PMOS transistor’s threshold voltage degradation $\Delta V_{th}(t)$ at any time t of its service life using our variation-aware NBTI model (described in the next section).

Next, we describe how to get a system’s service lifetime with $\Delta V_{th}(t)$. According to [12], the delay degradation of a gate v due to $\Delta V_{th}(t)$ can be approximately estimated as:

$$\Delta d(v, t) = \frac{\beta \Delta V_{th}(t)}{V_g - V_{th0}} \times d(v), \quad (1)$$

where β is the velocity saturation index, whose value ranges from 1 to 2. ΔV_{th0} is the original transistor threshold voltage and $d(v)$ is the fresh delay of gate v . If there are multiple threshold voltage degradations in the gate, we simply use the largest $\Delta V_{th}(t)$ to obtain the worst-case delay degradation.

The path delay degradation can be computed as the sum of delay degradation of all gates in the path. So the degradation of a path consisting of k gates is given as:

$$\Delta D(t) = \sum_{v=1}^k \Delta d(v, t). \quad (2)$$

In order to estimate the system’s service life, we conduct static timing analysis and choose those paths with guardbands less than a user-defined parameter. With Eq. 2, we can predict PCPs’ delay degradation at any time of system’s service lifetime. According to the amount of PCPs’ delay degradation and PCPs’ slacks, we can easily predict when timing violations would occur. System lifetime is defined as the time when the first timing error happens for PCPs.

Needless to say, the key challenge is to represent the transistor-level NBTI-induced degradation under various time-varying parameters (e.g., temperature and voltage) with extract time-independent parameter Ω , which is demonstrated in the next section.

4. VARIATION-AWARE NBTI MODELING IN TRANSISTOR LEVEL

According to earlier discussions, the key issue to estimate the system service life is to strip the time-varying factors from NBTI-induced degradation model and deduct a time independent degradation rate Ω that can be effectively extracted with limited traced information. This problem is challenging because, on the one hand, device stresses, as well as the NBTI degradation in different time intervals are not additive. On the other hand, an accurate model must capture the multiple sequences of stress and recovery events [8]. This section shows

how to achieve this objective using mathematical analysis. We tackle this problem in two steps. After deducting a close-form NBTI degradation function with system’s time-varying operational states (section 4.1), we transform the temperature variation into a constant temperature by scaling the time interval (Section 4.2). Next, we scale the time interval again to preserve the continuity of NBTI-induced degradation during operational state transition (Section 4.3). We further discuss the accuracy of the proposed model with different stress and recovery events in Section 4.4.

4.1 Close-Form NBTI Degradation

In [10], the authors proposed a long-term NBTI model, which provides an analytical upper bound of NBTI impact on PMOS transistor threshold voltage degradation over time. It can be described as follows:

$$\Delta V_{th}(t) = \left(\frac{\sqrt{K_v^2 \alpha T_{clk}}}{1 - \beta_t^{1/2n}} \right)^{2n}, \quad (3)$$

where

$$\beta_t = 1 - \frac{2\xi_1 t_e + \sqrt{\xi_2 C (1 - \alpha) T_{clk}}}{2t_{ox} + \sqrt{Ct}}, \quad (4)$$

and n is a constant based on diffusion species. α is the duty cycle or stress probability, T_{clk} is the clock period of stress and recovery phase, C covers temperature impact, t_{ox} is gate oxide thickness. For detailed parameters explanations, please refer to [10].

However, this analytical model was derived under the assumption that environment parameters like temperature and supply voltage remain constant. Therefore, we strip time t from above long term NBTI-induced degradation considering arbitrary temperature and voltage variations. Since gate oxide thickness t_{ox} is very small for today’s CMOS technology (e.g., it is only 1nm for 32nm technology [18]), for the long term effect, we assume $\sqrt{Ct} \gg 2t_{ox}$. When t is large enough (e.g., $t > 100s$), using the first order Taylor series approximation method, the long term degradation model can be simplified as

$$\Delta V_{th}(t) = \varphi t^n, \quad (5)$$

where

$$\varphi = \left[\frac{2n\sqrt{K_v^2 \alpha C T_{clk}}}{2\xi_1 t_e + \sqrt{\xi_2 C (1 - \alpha) T_{clk}}} \right]^{2n}. \quad (6)$$

φ covers system reliability-related factors such as supply voltage, temperature, frequency, duty cycle and also technology related parameters (e.g., gate oxide thickness). Our ultimate goal is to represent the long-term NBTI degradation in a form similar to Eq.5 and remove the effect of temperature and voltage variations from φ .

4.2 Transformation for stripping the time-varying factor in Temperature

[11] proposed a model that considers temperature impact by scaling time domain to make the threshold voltage degradation additive. However, this method is not directly applicable in the presence of voltage and frequency variations, which makes the analysis more complicated compared with only the temperature variation. Besides, our purpose is to obtain an analytical model suitable for efficient simulation. If we use the method in [11] to estimate system lifetime, we have to do the simulation for the whole lifetime, which is not possible.

Different from above method, we propose to transform the temperature variation by fixing the voltage, leveraging the DVFS policy. With DVFS policy, modern processors often have

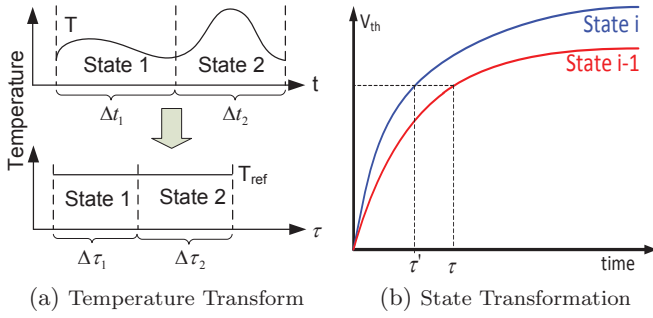


Figure 3: Transformation by Time Domain Scaling.

several execution states with different supply voltages or frequencies. So we characterize processors' execution states with different supply voltages or frequencies. When processors work from 0 to t , it may have several execution states. We assume it has m states, each state i lasts $\Delta t_i = t_i - t_{i-1}$ ($i = 1, 2, \dots, m$), which corresponds to an unique temperature distribution with maximum and minimum temperature $T_{max,i}$ and $T_{min,i}$. The corresponding supply voltage, frequency and duty cycle are V_i , f_i and α_i , respectively.

In each state, the supply voltage is constant, so we can use the method in [11] directly. We transform temperature variation effect into constant reference temperature effect by scaling time domain (e.g., $\Delta t_1 \Rightarrow \Delta \tau_1$ as shown in Fig. 3(a)). After that, the equivalent time of state i is

$$\Delta \tau_i = \int_{t_{i-1}}^{t_i} e^{[E_a/k] \cdot [1/T_{ref} - 1/T(t)]} dt. \quad (7)$$

In Eq. 7, T_{ref} is the reference temperature, E_a is the temperature activation energy, k is the Boltzman constant and $T(t)$ is the instantaneous temperature at time t . Assume $\rho(T) dT$ is the accumulated time in an infinitesimal temperature interval dT around T in state i , we use it to substitute dt , and obtain

$$\Delta \tau_i = \int_{T_{min,i}}^{T_{max,i}} e^{[E_a/k] \cdot [1/T_{ref} - 1/T(t)]} \rho(T) dT. \quad (8)$$

If the probability of the processor in state i is η_i , and $p_i(T)$ is the probability density function of temperature T at state i , then

$$\rho(T) = \eta_i \cdot p_i(T) \cdot t. \quad (9)$$

So the equivalent time of state i is as follows:

$$\Delta \tau_i = R_i \cdot t, \quad (10)$$

where

$$R_i = \int_{T_{min,i}}^{T_{max,i}} e^{[E_a/k] \cdot [1/T_{ref} - 1/T]} \eta_i p_i(T) dT. \quad (11)$$

It scales the original state duration based on the temperature distribution in the state. Its value can be easily obtained based on the traced information (e.g., the probability of state i and its temperature distribution) from the simulation.

Accordingly, in the τ domain, the original clock period $T_{clk,i}$ and duty cycle α_i in state i may correspond to different equivalent clock period $\hat{T}_{clk,i}$ and duty cycle $\hat{\alpha}_i$, which have the same forms as in [11].

4.3 Transformation for striping the time-varying factor from Voltage/Frequency

After transforming time from t domain to τ domain within each state, in this subsection, we subsequently transform the voltage variation among successive execution states.

In the τ domain, the degradation function Eq. 5 can still be preserved in each state. φ_i ($i = 1, 2, \dots, m$) corresponds to the constant temperature T_{ref} , supply voltage V_i , frequency \hat{f}_i and duty cycle $\hat{\alpha}_i$.

After first state, the threshold voltage degradation is

$$\Delta V_{th,1} = \varphi_1 \Delta \tau_1^n. \quad (12)$$

It should be noted that this equation will underestimate the degradation if $\Delta \tau_1$ is too short for using Eq. 5. However, the effect is too small to be counted. We can explain as this: if we do not distinguish processors' states until the Eq. 5 can be used, that is to say, we assume the first state lasts very long (e.g., lasts 100s, ignore the supply voltage/frequency changes in the first 100s), and calculate the effect of this assumption. Consider two supply voltages, V_{dd} and $0.8V_{dd}$, the maximum relative error the assumption causes for 10000s degradation is less than 0.1% based on our experimental results. So we can safely ignore this effect for long term (e.g., several years) PMOS threshold voltage degradation estimation.

Next we consider threshold voltage degradation after state i ($i > 1$). The change in φ between consecutive states causes discontinuity of threshold voltage degradation. See Fig. 3(b), when the processor changes state $i-1$ to i at time τ , in order to preserve the continuity of threshold voltage degradation, the duration of previous time should be adjusted to τ' , which means the threshold voltage degradation at the end of state $i-1$ must be the same as that at the beginning of state i . So the following function must be satisfied:

$$\Delta V_{th,i-1} = \varphi_i \tau'^n. \quad (13)$$

Then the threshold voltage degradation after state i is

$$\Delta V_{th,i} = \varphi_i \left[\left(\frac{\Delta V_{th,i-1}}{\varphi_i} \right)^{1/n} + \Delta \tau_i \right]^n. \quad (14)$$

Using Eq. 12 and Eq. 14, we can obtain $\Delta V_{th,m}$ as a function of $\Delta V_{th,m-1}$ and then repeatedly replacing $\Delta V_{th,i}$ by $\Delta V_{th,i-1}$ for $i = m, \dots, 1$, so the total threshold voltage degradation after t is

$$\Delta V_{th}(t) = \Delta V_{th,m} = \left(\sum_{i=1}^m \varphi_i^{1/n} \Delta \tau_i \right)^n. \quad (15)$$

Substitute $\Delta \tau_1, \Delta \tau_2, \dots, \Delta \tau_m$ into Eq. 15, the threshold voltage degradation from 0 to t can be written as follows:

$$\Delta V_{th}(t) = \Omega \cdot t^n, \quad (16)$$

where

$$\Omega = \left(\sum_{i=1}^m \varphi_i^{1/n} R_i \right)^n. \quad (17)$$

Now we have obtained a time-independent quantity Ω that can be used to calculate threshold voltage degradation. It relies on the probability of each execution state and the corresponding temperature distribution and duty cycle. We define Ω as degradation rate of PMOS transistor. If the processor has m states, the degradation rate Ω of each PMOS transistor threshold voltage degradation can be computed as Eq. 17.

In addition, if the system has multiple representative workloads, we can easily extend our model to cover this situation. If the probability of representative workload j is κ_j and the corresponding degradation rate is Ω_j , similar to the above deduction, the unified degradation rate of PMOS transistor is

$$\Omega = \left(\sum_j \Omega_j^{1/n} \kappa_j \right)^n. \quad (18)$$

4.4 Case Study: Varying the Sequences of Different Execution States

The above model is derived by estimating the occurrence probability of each execution state (supply voltage) in the service life (η_i in Eq. 9). One may doubt the accuracy because the sequence of the execution states may affect NBTI degradation. Consider four execution states with four supply voltages respectively: V_{dd} , $0.9V_{dd}$, $0.8V_{dd}$ and $0.7V_{dd}$. Two different sequences of execution states exist: (a) we apply V_{dd} first, then $0.9V_{dd}$, $0.8V_{dd}$, $0.7V_{dd}$ and then V_{dd} again and so on; (b) we apply $0.9V_{dd}$ first, then V_{dd} , $0.7V_{dd}$, $0.8V_{dd}$ and then $0.9V_{dd}$ again and so on. To study the impact of voltage sequences, we simulate the above two schemes using cycle accurate model [10]. It should be noted that, the voltage is the only concern in this study. Because the temperature variation is almost the same between above two schemes. Consequently, we can set the temperature as a constant and assume each cycle lasts 0.1s. We change the execution state every p seconds with p varying from 0.1s to 3600s for common DVFS policy. We find that the difference of degradation is minor between above two schemes. And the maximum difference of degradation between the two schemes is less than 0.9% for 5-year service life. When p is extremely large (e.g., about 1 to 2 years), the voltage sequences have a significant effect on the degradation. However, these extreme cases rarely exist in realistic. Consequently, it is acceptable for our model to exclude the effect of execution sequences by only considering their occurrence probabilities.

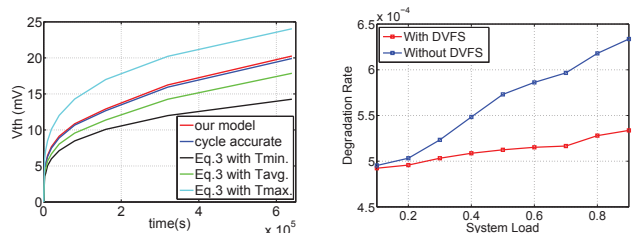
5. EXPERIMENTAL RESULTS

In this section, we first validate our model and then present the simulation results based on our proposed framework. The target system used in our experiment is OpenRISC OR1200 [19]. The model parameters in our experiments are from [10] and [18]. Due to the lack of public benchmark workloads to estimate aging effects, we present separate synthetic workloads for our simulation as follow: we first run the benchmark workloads provided by [19] and then use them as atomic workloads to randomly generate a large number of applications in such a manner that the application’s reliability-related information (e.g., power, stress probability) conform to that obtained when running atomic workloads. The application arrival to the system is assumed to be a Poisson process with arrival rate λ . And the service time of the system is an exponential distribution with mean $1/\mu$. System load ρ can be derived by λ/μ . Clearly, higher ρ means the system has more workloads to process. When using our model and framework, designers should provide such kinds of workload information.

5.1 Model Validation

To the best of our knowledge, NBTI effects with temperature and supply voltage variations for real systems have not been reported in the literature. In order to validate our model, we compare it with the cycle-accurate degradation model proposed in [10], which has been validated by measurement data. As long as the threshold voltage degradation obtained from our model conforms to the one by running simulation cycle by cycle, our model is verified. For the above models, we fix the frequency and trace the temperature by HotSpot simulation. We also use the minimum, average and maximum temperatures to calculate the degradation based on the original long term degradation model Eq. 3.

Fig. 4(a) presents the threshold voltage degradation calculated using the above models in a range of 0s to 6×10^5 s simulation. The results show that the proposed model can achieve almost identical threshold voltage degradation compared to the cycle-accurate model for a long time of simulation. The maximum error between our model and the cycle-accurate



(a) Accuracy Comparison.

(b) DVFS Impact

Figure 4: Transistor Level Simulation.

model is less than 1.5%. However, the maximum errors of the original long term degradation model using minimum, average and maximum temperatures are 35.9%, 14.2% and 28.3%, respectively. For the analytical model without considering the temperature variation, it obviously results in significant errors. And this can justify the necessity of considering time-varying parameters in order to obtain accurate prediction.

5.2 The Impact of DVFS

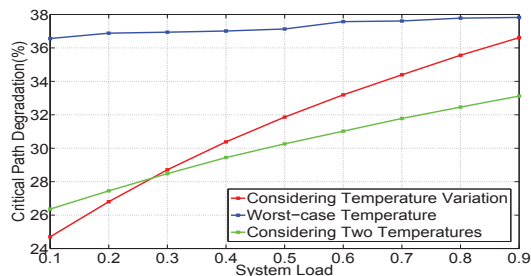
During system operation, we assume that the processor core can be in one of four states with DVFS: high voltage run, high voltage idle, low voltage run and low voltage idle. In our experiment, the high voltage corresponds to V_{dd} , the low voltage corresponds to $0.8V_{dd}$. We use the same DVFS strategy as from [15]: when the highest/lowest temperature of the processor is higher/lower than the threshold temperature T_H/T_L , it decreases/increases its supply voltage or frequency. We assume the transition time between states is zero and set $T_H = 353.15K$ and $T_L = 343.15K$.

Fig. 4(b) shows a PMOS transistor’s degradation rate under two conditions (with and without DVFS respectively) by varying the system loads. As the system load increases, PMOS degradation rate under both conditions increase as well. When the system load is small, we observe that the degradation rate with DVFS increases slightly slower than that without DVFS. That is because, the temperature accumulated in the system is not high enough to trigger the DVFS, and therefore the system spends most of the time in high voltage active or high voltage idle. As the system load becomes larger, the degradation rate with DVFS increases much slower than that without DVFS. Because the temperature breaks through the threshold temperature T_H more frequently, rendering the DVFS more effective. Thus, the portion of low voltage in the system service life increases, which slows down NBTI-induced degradation.

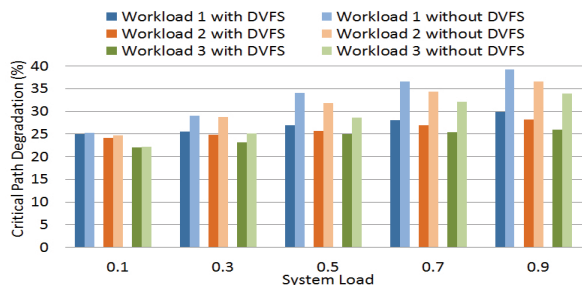
5.3 System Performance Degradation

Next, we use our framework to estimate system performance degradation. Since NBTI only affects PCPs, if the functional block does not contain PCPs (e.g., WISHBONE BIU block), we do not have to analyze it. When analyzing a functional block, we pick those paths with timing slacks less than 40% guardbands as the PCPs and use our model to predict the performance degradation after 10 years operation.

To deal with NBTI-induced performance degradation, designers often analyze the system by assuming the worst-case temperature and set a conservative guardband for critical paths. Fig. 5(a) shows the degradation of the critical paths using our simulation framework comparing to that using long-term degradation model [10] with a constant worst-case temperature. We also present the degradation derived from the model proposed in [12] by considering two temperatures for active and idle states. We find that the predicted degradation based on the worst-case is as high as 36% and remains almost the same with different system loads. A possible explanation is that, with the constant worst-case temperature, the system can quickly accumulate a very high temperature as long as the workloads begin to execute. This is obviously too pessimistic



(a) Temperature Impact



(b) Impact of DVFS and Workloads

Figure 5: Simulation on System Performance (Critical Path) Degradation after Ten Years Operation.

because, only in rare cases, a workload (or several workloads) can generate such a high temperature. Moreover, if the worst-case temperature is similar under different system load, the degradation remains even the system load increases. The degradation estimated by our model gradually ascends as system load increases. The amount of degradation is about 10% less compared to the worst-case scenario when the system load is light and is about 1% less when the system load is high. This is reasonable because our model reveal the fact that the system have more idle times to cool down the temperature when the system load is light. However, when the system load is too high, the system will remain a high temperature (close to the worst-case one) that leads to severe degradation.

The model considering only two temperatures predicts a different degradation trend, wherein the degradation at high system load is less than that predicted by our model. We believe this two-temperature model under-estimates the degradation because it assumes the temperature can drop instantly when the system becomes idle. In reality, it is more difficult for a system to cool down when the system load becomes larger. That is why we can see the degradation predicted by our model is more severe at high system load comparing to that predicted by the two-temperature model. We can deduct that the two-temperature model over-estimates the degradation at light system load in a similar way.

We use different atomic workloads as the representative workloads. Fig. 5(b) gives the critical path degradation after 10 years under the impact of DVFS and different representative workloads. We can see that different representative workloads indeed will affect the critical path degradation. This is because workloads not only affect the circuits utilization, but also have an impact on bit patterns for circuits. The workloads doing floating point operations will certainly affect the degradation of paths in the floating point unit of the processor. Other workloads without floating point operations do not have much impact on the degradation of these paths, since the block is always idle in these cases. In practice, designers need to provide different representative workloads for the target system when using our model and framework. Under DVFS, the critical path degrades slower than that without DVFS, which is similar with its effect on single PMOS degradation. It should be noted that, some previous works show that non-critical path can become critical due to NBTI effect, but we have not observed this phenomenon in our experiments.

6. CONCLUSION

In this paper, we propose a comprehensive NBTI degradation model considering arbitrary temperature and voltage variations. Then, based on the proposed model, we present an efficient simulation framework for system lifetime prediction by running representative workloads. As shown in our experimental results, the proposed solution is more accurate than previous solutions.

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